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**Engineering : Circuits and Systems**

Ho, Ron, Drost, Robert (Eds.)

# Coupled Data Communication Techniques for High-Performance and Low-Power Computing

- Serves as a collection of the best-known-methods and ideas from leaders in the field.
- Includes a carefully-selected set of discussions on the important issues, tradeoffs, and techniques in coupled data I/O.
- Provides an overview of the circuits, architectures, and chip packaging for coupled data techniques.
- Covers the new and emerging area of coupled data communication.

Wafer-scale integration has long been the dream of system designers. Instead of chopping a wafer into a few hundred or a few thousand chips, one would just connect the circuits on the entire wafer. What an enormous capability wafer-scale integration would offer: all those millions of circuits connected by high-speed on-chip wires. Unfortunately, the best known optical systems can provide suitably fine resolution only over an area much smaller than a whole wafer. There is no known way to pattern a whole wafer with transistors and wires small enough for modern circuits. Statistical defects present a former barrier to wafer-scale integration. Flaws appear regularly in integrated circuits; the larger the circuit area, the more probable there is a flaw. If such flaws were the result only of dust one might reduce their numbers, but flaws are also the inevitable result of small scale. Each feature on a modern integrated circuit is carved out by only a small number of photons in the lithographic process. Each transistor gets its electrical properties from only a small number of impurity atoms in its tiny area. Inevitably, the quantized nature of light and the atomic nature of matter produce statistical variations in both the number of photons defining each tiny shape and the number of atoms providing the electrical behavior of tiny transistors.

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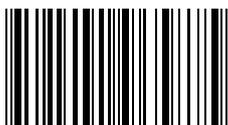
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