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Chang, K.-h., Markov, I.L., Bertacco, V.

Functional Design Errors in Digital Circuits

Diagnosis Correction and Repair

- Coverage of novel techniques to automate IC debugging, a subject rarely covered in other books
- Comprehensive scope and solutions: from RTL to post-silicon debugging
- The innovative techniques covered in this book are recent and have been featured by MIT Technology Review, EE Times, SCD Source, IEEE Computer, and other sources
- First empirical comparison of several methods for spare-cell insertion
- A variety of examples and figures to illustrate key concepts and algorithms

Functional Design Errors in Digital Circuits Diagnosis covers a wide spectrum of innovative methods to automate the debugging process throughout the design flow: from Register-Transfer Level (RTL) all the way to the silicon die. In particular, this book describes: (1) techniques for bug trace minimization that simplify debugging; (2) an RTL error diagnosis method that identifies the root cause of errors directly; (3) a counterexample-guided error-repair framework to automatically fix errors in gate-level and RTL designs; (4) a symmetry-based rewiring technology for fixing electrical errors; (5) an incremental verification system for physical synthesis; and (6) an integrated framework for post-silicon debugging and layout repair. The solutions provided in this book can greatly reduce debugging effort, enhance design quality, and ultimately enable the design and manufacture of more reliable electronic devices.

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