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Generating Hardware Assertion Checkers

For Hardware Verification, Emulation, Post-Fabrication Debugging and On-Line Monitoring

- Efficient synthesis of assertion checkers for the main assertion languages (PSL and SVA)
- Applications in verification, emulation, post-fabrication debugging, on-line monitoring, with a unique “under-the-hood” view
- A missing link between the literature on assertion languages and pre-made checker libraries
- Extensive benchmarks and verification of assertion checkers, with examples of real-world circuit checkers
- Comprehensive background on hardware assertion languages, temporal logic and finite automata

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Assertion-based design is a powerful new paradigm that is facilitating quality improvement in electronic design. Assertions are statements used to describe properties of the design (I.e., design intent), that can be included to actively check correctness throughout the design cycle and even the lifecycle of the product. With the appearance of two new languages, PSL and SVA, assertions have already started to improve verification quality and productivity. This is the first book that presents an “under-the-hood” view of generating assertion checkers, and as such provides a unique and consistent perspective on employing assertions in major areas, such as: specification, verification, debugging, on-line monitoring and design quality improvement.

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