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System-on-Chip Security

Validation and Verification

- Outlines a wide variety of hardware security threats and vulnerabilities as well as their sources in each of the stages of a design life cycle
- Summarizes unsafe current design practices that lead to security and trust vulnerabilities
- Covers state-of-the-art techniques as well as ongoing research efforts in developing scalable security validation using formal methods including symbolic algebra, model checkers, SAT solvers, and theorem provers
- Explains how to leverage security validation approaches to prevent side-channel attacks
- Presents automated debugging and patching techniques in the presence of security vulnerabilities

This book describes a wide variety of System-on-Chip (SoC) security threats and vulnerabilities, as well as their sources, in each stage of a design life cycle. The authors discuss a wide variety of state-of-the-art security verification and validation approaches such as formal methods and side-channel analysis, as well as simulation-based security and trust validation approaches. This book provides a comprehensive reference for system on chip designers and verification and validation engineers interested in verifying security and trust of heterogeneous SoCs.

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