Contents

Digital Design

Flexible Composite Galois Field $GF((2^m)^2)$ Multiplier Designs . . . . . . . . . . 3
  M. Mohamed Asan Basiri and Sandeep K. Shukla

Estimating the Maximum Propagation Delay of 4-bit Ripple Carry Adder Using Reduced Input Transitions. .......................... 15
  Manan Mewada, Mazad Zaveri, and Anurag Lakhani

VLSI Implementation of Throughput Efficient Distributed Arithmetic Based LMS Adaptive Filter ........................................... 24
  Mohd. Tasleem Khan and Shaik Rafi Ahamed

Realization of Multiplier Using Delay Efficient Cyclic Redundant Adder . . . . . . . . . . . 36
  K. Dheepika, K. S. Jevasankari, Vippin Chandhar, and Binsu J. Kailath

Fast Architecture of Modular Inversion Using Itoh-Tsujii Algorithm . . . . . . 48
  Pravin Zode, R. B. Deshmukh, and Abdus Samad

Performance Optimized 64b/66b Line Encoding Technique for High Speed SERDES Devices .................................................. 56
  Jatindeep Singh, Satyajit Mohapatra, and Nihar Ranjan Mohapatra

A New Multi-objective Hardware-Software-Partitioning Algorithmic Approach for High Speed Applications ................................ 62
  Naman Govil, Rahul Shrestha, and Shubhajit Roy Chowdhury

A Framework for Branch Predictor Selection with Aggregation on Multiple Parameters ............................................................ 69
  Moumita Das, Ansuman Banerjee, and Bhaskar Sardar

FPGA Implementation of a Novel Area Efficient FFT Scheme Using Mixed Radix FFT ................................................................ 75
  Thilagavathy R, Susmitha Settivari, Venkataramani B, and Bhaskar M

Analog/Mixed Signal

Low Voltage, Low Power Transconductor for Low Frequency
$G_m$-C Filters ........................................................................................................................................................................ 83
  Hanumantha Rao G. and Rekha S.
An Improved Highly Efficient Low Input Voltage Charge Pump Circuit 93
Naresh Kumar, Raja Hari Gudlavalleti, and Subash Chandra Bose

A Calibration Technique for Current Steering DACs - Self Calibration with Capacitor Storage 103
Pallavi Darji and Chetan Parikh

Characterization and Compensation Circuitry for Piezo-Resistive Pressure Sensor to Accommodate Temperature Induced Variation 115
M. Santosh, Anjli Bansal, Jitendra Mishra, K. C. Behra, and S. C. Bose

FEM Based Device Simulator for High Voltage Devices 127
Ashok Ray, Gaurav Kumar, Sushanta Bordoloi, Dheeraj Kumar Sinha, Pratima Agarwal, and Gaurav Trivedi

Synapse Circuits Implementation and Analysis in 180 nm MOSFET and CNFET Technology 136
Sushma Srivastava and S. S. Rathod

A 10 MHz, 73 ppm/°C, 84 μW PVT Compensated Ring Oscillator 144
Vivek Tyagi, M. S. Hashmi, Ganesh Raj, and Vikas Rana

VLSI Testing

Deterministic Shift Power Reduction in Test Compression 155
Kanad Basu, Rishi Kumar, Santosh Kulkarni, and Rohit Kapur

Pseudo-BIST: A Novel Technique for SAR-ADC Testing 168
Yatharth Gupta, Sujay Deb, Vikrant Singh, V. N. Srinivasan, Manish Sharma, and Sabyasachi Das

SFG Based Fault Simulation of Linear Analog Circuits Using Fault Classification and Sensitivity Analysis 179
Rahul Bhattacharya, S. H. M. Ragamai, and Subindu Kumar

A Cost Effective Technique for Diagnosis of Scan Chain Faults 191
Satyadev Ahlawat, Darshit Vaghani, Jaynarayan Tudu, and Ashok Suhag

Multi-mode Toggle Random Access Scan to Minimize Test Application Time 205
Anshu Goel and Rohini Gulve
Performance Analysis of Disability Based Fault Tolerance Techniques for Permanent Faults in Chip Multiprocessors. Avishek Choudhury and Biplab K. Sikdar

Devices and Technology – I

Low-Power Sequential Circuit Design Using Work-Function Engineered FinFETs Ashish Soni, Abhijit Umap, and Nihar R. Mohapatra

Vertical Nanowire FET Based Standard Cell Design Employing Verilog-A Compact Model for Higher Performance Satish Maheshwaram, Om Prakash, Mohit Sharma, Anand Bulusu, and Sanjeev Manhas

Analysis of Electrolyte-Insulator-Semiconductor Tunnel Field-Effect Transistor as pH Sensor Ajay Singh, Rakhi Narang, Manoj Saxena, and Mridula Gupta

Exploiting Characteristics of Steep Slope Tunnel Transistors Towards Energy Efficient and Reliable Buffer Designs for IoT SoCs Japa Aditya, Vallabhaneni Harshita, and Ramesh Vaddi

An Efficient VLSI Architecture for PRESENT Block Cipher and Its FPGA Implementation Jai Gopal Pandey, Tarun Goel, and Abhijit Karmakar

Investigation of TCADs Models for Characterization of Sub 16 nm In$_{0.53}$Ga$_{0.47}$As FinFET J. Pathak and A. Darji

Hausdorff Distance Driven L-Shape Matching Based Layout Decomposition for E-Beam Lithography Arindam Sinharay, Pranab Roy, and Hafizur Rahaman

VLSI Architectures

Energy-Efficient VLSI Architecture & Implementation of Bi-modal Multi-banked Register-File Organization Sumanth Gudaparthi and Rahul Shrestha

Performance-Enhanced $d^2$-LBDR for 2D Mesh Network-on-Chip Anugrah Jain, Vijay Laxmi, Meenakshi Tripathi, Manoj Singh Gaur, and Rimpy Bishnoi
ACAM: Application Aware Adaptive Cache Management for Shared LLC . . 324
  Sujit Kr Mahto and Newton

Adaptive Packet Throttling Technique for Congestion Management
in Mesh NoCs .................................................. 337
  N. S. Aswathy, R. S. Reshma Raj, Abhijit Das, John Jose,
  and V. R. Josna

Defeating HaTCh: Building Malicious IP Cores ......................... 345
  Anshu Bhardwaj and Subir Kumar Roy

Low Cost Circuit Level Implementation of PRESENT-80 S-BOX ........... 354
  S. Shanthi Rekha and P. Saravanan

**Emerging Technologies and Memory**

Modeling and Analysis of Transient Heat for 3D IC ..................... 365
  Subhajit Chatterjee, Surajit Kr. Roy, Chandan Giri,
  and Hafizur Rahaman

Memory Efficient Fractal-SPIHT Based Hybrid Image Encoder ........... 376
  Mamata Panigrahy, Nirmal Chandra Behera, B. Vandana,
  Indrajit Chakrabarti, and Anindya Sundar Dhar

Metal-Oxide Nanostructures Designed by Glancing Angle Deposition
Technique and Its Applications on Sensors and Optoelectronic Devices:
A Review ......................................................... 388
  Divya Singh

Low Write Energy STT-MRAM Cell Using 2T- Hybrid Tunnel FETs
Exploiting the Steep Slope and Ambipolar Characteristics .............. 398
  Y. Sudha Vani, N. Usha Rani, and Ramesh Vaddi

Enhancing Retention Voltage for SRAM ................................ 406
  Ankit Rehani, Sujay Deb, and Suprateek Shukla

Comparison of SRAM Cell Layout Topologies to Estimate Improvement
in SER Robustness in 28FDSOI and 40 nm Technologies .................. 414
  Anand Ilakal and Anuj Grover

Improving the Design of Nearest Neighbor Quantum Circuits in 2D Space . 421
  Neha Chaudhuri, Chandan Bandyopadhyay, and Hafizur Rahaman

**Devices and Technology – II**

Delay and Frequency Investigations in Coupled MLGNR Interconnects ..... 429
  Manish Joshi, Koduri Teja, Ashish Singh, and Rohit Dhiman
LISOCHIN: An NBTI Degradation Monitoring Sensor for Reliable CMOS Circuits ......................................................... 441
  Ambika Prasad Shah, Nandakishor Yadav, and Santosh Kumar Vishvakarma

Performance Analysis of OLED with Hole Block Layer and Impact of Multiple Hole Block Layer. ........................................ 452
  Shubham Negi, Poornima Mittal, and Brijesh Kumar

Improved Gate Modulation in Tunnel Field Effect Transistors with Non-rectangular Tapered Y-Gate Geometry....................... 463
  Rakhi Narang, Mridula Gupta, and Manoj Saxena

A 36 nW Power Management Unit for Solar Energy Harvesters Using 0.18 µm CMOS .......................................................... 474
  Purvi Patel, Biswajit Mishra, and Dipankar Nagchoudhuri

A 10T Subthreshold SRAM Cell with Minimal Bitline Switching for Ultra-Low Power Applications ........................................ 487
  Swaanti and Bishnu Prasad Das

Variability Investigation of Double Gate JunctionLess (DG-JL) Transistor for Circuit Design Perspective ................................. 496
  Vandana Kumari, Manoj Saxena, and Mridula Gupta

System Design

A High Speed KECCAK Coprocessor for Partitioned NSP Architecture on FPGA Platform .................................................. 507
  Rourab Paul and Sandeep Kumar Shukla

New Energy Efficient Reconfigurable FIR Filter Architecture and Its VLSI Implementation .............................................. 519
  Naushad Ali and Bharat Garg

FPGA-Based Smart Camera System for Real-Time Automated Video Surveillance ................................................. 533
  Sanjay Singh, Sumeet Saurav, Ravi Saini, Atanendu S. Mandal, and Santanu Chaudhury

Effectiveness of High Permittivity Spacer for Underlap Regions of Wavy-Junctionless FinFET at 22 nm Node and Scaling Short Channel Effects ............................................................... 545
<table>
<thead>
<tr>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design and Implementation of Ternary Content Addressable Memory</td>
<td>557</td>
</tr>
<tr>
<td>(TCAM) Based Hierarchical Motion Estimation for Video Processing</td>
<td></td>
</tr>
<tr>
<td><em>Puja Ghosh and P. Rangababu</em></td>
<td></td>
</tr>
<tr>
<td>A Custom Designed RISC-V ISA Compatible Processor for SoC</td>
<td>570</td>
</tr>
<tr>
<td><em>Kavya Sharat, Sumeet Bandishte, Kuruvilla Varghese, and Amrutur Bharadwaj</em></td>
<td></td>
</tr>
<tr>
<td><strong>Low Power Design and Test</strong></td>
<td></td>
</tr>
<tr>
<td>An Efficient Timing and Clock Tree Aware Placement Flow</td>
<td>581</td>
</tr>
<tr>
<td>with Multibit Flip-Flops for Power Reduction</td>
<td></td>
</tr>
<tr>
<td><em>Jasmine Kaur Gulati, Bhanu Prakash, and Sumit Darak</em></td>
<td></td>
</tr>
<tr>
<td>Primitive Instantiation Based Fault Localization Circuitry</td>
<td>594</td>
</tr>
<tr>
<td>for High Performance FPGA Designs</td>
<td></td>
</tr>
<tr>
<td><em>Ayan Palchaudhuri and Anindya Sundar Dhar</em></td>
<td></td>
</tr>
<tr>
<td>On Generation of Delay Test with Capture Power Safety</td>
<td>607</td>
</tr>
<tr>
<td><em>Rohini Gulve and Nihar Hage</em></td>
<td></td>
</tr>
<tr>
<td>A Configurable and Area Efficient Technique for Implementing</td>
<td>619</td>
</tr>
<tr>
<td>Isolation Cells in Low Power SoC</td>
<td></td>
</tr>
<tr>
<td><em>Prokash Ghosh and Jyotirmoy Ghosh</em></td>
<td></td>
</tr>
<tr>
<td><strong>RF Circuits</strong></td>
<td></td>
</tr>
<tr>
<td>A 10 MHz, 42 ppm/°C, 69 μW PVT Compensated Latch Based Oscillator</td>
<td>631</td>
</tr>
<tr>
<td>in BCD9S Technology for PCM</td>
<td></td>
</tr>
<tr>
<td><em>Vivek Tyagi, M. S. Hashmi, Ganesh Raj, and Vikas Rana</em></td>
<td></td>
</tr>
<tr>
<td>A 1.8 V Gain Enhanced Fully Differential Doubly-Recycled Cascode</td>
<td>646</td>
</tr>
<tr>
<td>OTA with 100 dB Gain 200 MHz UGB in CMOS</td>
<td></td>
</tr>
<tr>
<td><em>Antaryami Panigrahi and Abhipsa Parhi</em></td>
<td></td>
</tr>
<tr>
<td>A Low Power, Frequency-to-Digital Converter CMOS Based Temperature</td>
<td>657</td>
</tr>
<tr>
<td>Sensor in 65 nm Process</td>
<td></td>
</tr>
<tr>
<td><em>Mudasir Bashir, Sreehari Rao Patri, and K. S. R. Krishna Prasad</em></td>
<td></td>
</tr>
<tr>
<td>Design &amp; Development of High Speed LVDS Receiver with Cold-Spare</td>
<td>667</td>
</tr>
<tr>
<td>Feature in SCL’s 0.18 μm CMOS Process</td>
<td></td>
</tr>
<tr>
<td><em>Munish Malik, Ajay Kumar, and H. S. Jatana</em></td>
<td></td>
</tr>
<tr>
<td><strong>Architecture and CAD</strong></td>
<td></td>
</tr>
<tr>
<td>Fast FPGA Placement Using Analytical Optimization</td>
<td>681</td>
</tr>
<tr>
<td><em>Sameer Pawanekar and Gaurav Trivedi</em></td>
<td></td>
</tr>
</tbody>
</table>