Preface

Memory technology has gained a pivotal position in the contemporary semiconductor computation industry. The last few decades have witnessed remarkable changes in the role and importance of various semiconductor memory technologies based on key parameters such as speed, power, density, and cost per bit of storage devices. The punch cards used in the beginning of the last century required an access time of nearly one second for the card of 1 KB memory size; on the contrary, modern finger-sized flash memories are able to achieve a speed of nearly Gbps. At present, modern computing systems employ magnetic memories such as hard disk drives (HDDs) and semiconductor memories such as static random access memory (SRAM), dynamic random access memory (DRAM), and flash memories at different levels of memory hierarchy.

In the diminishing era of Moore's law on the silicon road map, all the aforementioned memory technologies are still unable to cope with the speed of contemporary processing devices. Nonvolatile HDDs with high storage capacity are bulkier and sluggish; hence, they remain at the bottom of the memory hierarchy. At the top of the memory hierarchy, SRAM exhibits highest speed near to 1 ns; however, SRAM lacks in storage capacity, dissipates very high standby leakage power, and is volatile in nature. DRAM faces the problems of increasing refresh current and complex physical fabrication process. Flash memories suffer from excess write power, sluggish write speed, reliability and inadequate endurance issues. Therefore, it is imperative for the researchers to develop alternative nonvolatile memory technology solutions to meet the requirements of futuristic high-speed communication and computational applications. Emerging nonvolatile memory (NVM) technologies, including spin-torque magnetic RAM (ST-MRAM), ferroelectric RAM (FeRAM), phase change RAM (PCRAM), and resistive RAM (RRAM), are some of the competing and promising contenders as memory technologies for futuristic high-speed high-density on-chip storage applications.

Among all the aforementioned emerging NVM technologies, spintronic memory technologies have become the center of research attraction due to their possession of all the features of a universal memory such as nonvolatility, higher densities, enhanced performance, low power dissipation, unlimited endurance, high retention,

and CMOS-compatible fabrication process. This book describes all these facets of various spintronic-based magnetic memories such as spin transfer torque (STT), spin orbit torque (SOT), domain wall (DW) MRAMs, and sequential racetrack memories (RM). A spintronic device known as magnetic tunnel junction (MTJ) which utilizes the spin of electrons as a state variable is the key element in all kinds of emerging spintronic MRAMs. Specifically, perpendicular magnetic anisotropy (PMA)-based MTJ devices with their scalable architectures in the nanoscale regime and low-power magnetic switching requirements have gained stupendous interest among the research community. All these spintronic memories require an MTJ with one or two access transistors; hence, a huge footprint area saving can be achieved in comparison with conventional semiconductor memories.

In the initial phase of evolution, STT-MRAMs have encountered the problems of high switching threshold current and larger access device dimensions; however, with the advent of PMA devices, recently, the switching current requirements have been made low enough to reach at the level of 10 μA with access time near to the SRAMs which is best suitable for on-chip embedded memory applications. Significant efforts are being made to decrease the access device dimensions using metal oxide semiconductor (MOS) technologies other than the planar architectures with larger driving capabilities. This book describes the gate-all-around (GAA) MOSFET (MOS field effect transistor), a vertical 3-dimensional (3D) nanowire access device, employed to drive an MTJ element resulting an STT-MRAM with minimum footprint area of $4F^2$ (F is the feature size). SOT-MRAM provides the energy-efficient memory technology solution with different read and write path optimization. Multilevel-cell (MLC) MRAMs offer high density at reduced cost per bit with the help of series or parallel arrangements of the storage elements, i.e. MTJs. Racetrack memory utilizes the concept of magnetic domain wall motion within a nanowire and has the potential to cover the entire memory hierarchy. Racetrack memories (RM) possess all the features of a universal memory architecture, e.g., high density of HDD, high speed as SRAMs, unlimited endurance, high retention period, nonvolatility, lower switching and operation power, and above all capability of 3D integration with the complementary metal oxide semiconductor (CMOS)-compatible fabrication process. Therefore, RM can become a revolutionary memory technology which is best suitable for high-speed embedded communication and computing devices.

This book comprehensively describes all the aspects of the spintronic memories and discusses the importance of various key physical and electrical parameters affecting the performance of the memories to be considered while designing and optimizations. Chapter 1 provides a brief introduction to all the emerging spintronic memories covered in this book. Chapter 2 provides the detailed insight into next-generation 3D vertical silicon nanowire (NW)-based STT-MRAMs with vertical GAA select device. With the help of a case study, a performance comparison between GAA device based and planar MOSFET-based STT-MRAMs has been demonstrated. The evident advantages of GAA-based vertical silicon nanowire STT-MRAMs in terms of write margins, power dissipation, and 2D array density of $4F^2$ have been presented in the chapter. Chapter 3 provides a comprehensive

description of SOT-MRAM including the understanding of basic operational mechanisms and modeling of the same. A comparative performance analysis of STT- and SOT-MRAMs has been depicted at the end of the chapter. Chapter 4 demonstrates series and parallel configurations of the MLC MRAMs using in-plane magnetic anisotropy (IMA) and PMA MTJ devices. This chapter provides a detailed comparison of all the possible combinations of MLC structures with the help of simulations carried out using the SPICE-compatible simulation framework. Chapter 5 reveals the importance of most attractive and emerging racetrack memory technology which has the potential to revolutionize the computing industry. A fundamental concept of domain wall motion which is playing a key role in the racetrack memory is discussed broadly in the chapter. At the end the chapter, the important features of racetrack memory to realize the concept of "logic-in-memory" are discussed.

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