Chapter 2
Next Generation 3-D Spin Transfer Torque Magneto-resistive Random Access Memories

Spin transfer torque magneto-resistive random access memories (STT MRAMs) are non-volatile memories that potentially demonstrate high speed and integration density. These exclusive features of STT MRAMs are rapidly gaining attention of memory designers. They are strong contenders for futuristic embedded memory applications. However, further reduction in write power dissipation and cell size is essential to employ STT MRAMs for embedded applications. In most memory technologies, the select device has been the bottleneck towards increasing the array density [1]. Keeping this in mind, several novel architectures for select devices have been proposed by researchers working in the area [2–4]. They have been primarily focusing on vertical select devices to reduce the cell area. Kawahara et al. [5] suggested the possibility of a reduction in the cell area of spin transfer torque STT MRAMs down to $4F^2$ (F is the feature size) with a vertical select device. However, till date, the vertical select device could not be used in STT MRAM cells due to the requirement of high threshold switching current in the in-plane magnetic tunnel junction (MTJ) technology. The typical range of threshold switching current for conventional in-plane MTJs is 200–1200 μA [6, 7]. Such high current drive could not be achieved with minimum sized transistors, and hence, scaling towards $4F^2$ array density per cell was not feasible for STT MRAMs with in-plane MTJs. However, with the evolution of perpendicular magnetic anisotropy (PMA) MTJs which exhibit switching threshold of less than 100 μA [6], one can see decent prospects for higher array density in STT MRAMs.

In this chapter, the novel design of STT MRAMs on vertical silicon nano-wire (NW) platform is investigated. The chapter also discusses the architecture, operation and performance parameters of conventional STT MRAMs. Further, using extensive technology computer aided design (TCAD) and Hewlett simulation program with integrated circuit emphasis (HSPICE) simulations, the performance of STT MRAM with vertical gate-all-around (GAA) device is analyzed using a case study.

B.K. Kaushik et al., *Next Generation Spin Torque Memories*,
SpringerBriefs in Applied Sciences and Technology,
DOI 10.1007/978-981-10-2720-8_2

The chapter comprises of six sections including the current introductory section. The architecture and functionality of the conventional STT MRAM cell are presented in Sect. 2.1. Further, Sect. 2.2 compares the cell size in different volatile and non-volatile memory technologies. The Sect. 2.3 outlines the next generation $4F^2$ STT MRAM and the simulation framework used for analyzing STT MRAM cells. Section 2.4 presents a case study on the design of the next generation STT MRAM cell with vertical GAA select device. The case study includes a comprehensive TCAD analysis of the proposed buried source GAA device followed by analysis and comparison of the bit cell simulation results on HSPICE using calibrated Verilog-A models. A fabrication methodology of proposed STT MRAM cell on vertical silicon nano-wire (NW) platform is presented in Sect. 2.5. Finally, Sect. 2.6, concludes the chapter.

2.1 Overview of Conventional STT MRAM: Architecture and Operation

STT MRAMs have 3D integration of MTJs with conventional CMOS technology. The memory cell of STT MRAMs has one MTJ and one NMOS select device, abbreviated as a 1T-1MTJ cell. The structure and properties of a typical 1T-1MTJ STT MRAM cell can be understood through Fig. 2.1. The bottom layer (pinned or fixed layer) of an MTJ has fixed magnetization due to its comparatively high magnetic coercivity. The top layer of the MTJ is known as free/recording layer whose magnetization can be switched by the spin torque acting on it. This spin torque is generated by the electric current, which is spin polarized by the pinned bottom layer. The directions of current for writing 1 and 0 are shown in the Fig. 2.1. A current from bit line (BL) to source line (SL) would make the magnetization orientation as P (to write a 0). Conversely, a current from SL to BL would make the magnetization states of two layers as AP (to write a 1). Besides this, for both the directions, the write currents need to be above a minimum threshold value for

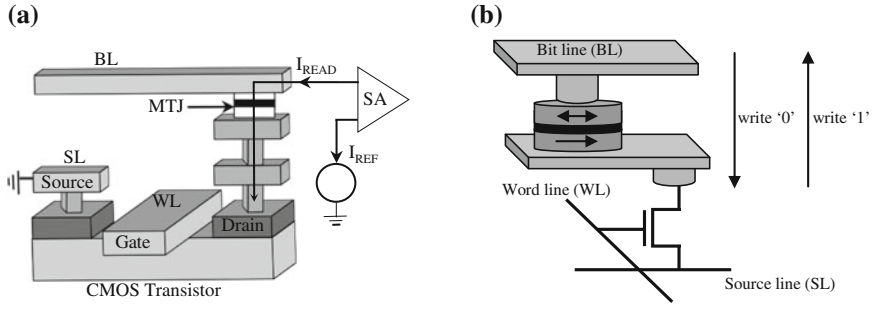

Fig. 2.1 **a** Typical integration of MTJ with CMOS technology in STT MRAM. **b** Write operation in STT MRAMs

proper switching of the MTJ. The minimum threshold value of current required for P(AP) to AP(P) switching is represented as $I_{LH0}(I_{HL0})$.

The data stored in MTJ is read by comparing current through MTJ with a reference resistance as shown in Fig. 2.1a. An optimum read voltage at BL is found by simultaneous consideration of *TMR* degradation effect with MTJ bias voltage and read current difference between P and AP states of MTJ [8]. Since, this read current has to be compared with a reference current to read the data, the difference in cell current between 0 and 1 stored cells should be high enough to be discernible.

In an MTJ, an interaction of spin polarized electrons with the local magnetic moment of FM layer takes place during which exchange of the spin angular momentum prompts to magnetization switching. For anti-parallel (AP or R_{AP}) to parallel (P or R_P) switching, the NMOS facilitates a current flow from the BL to SL as shown in Fig. 2.2a. Here, R_{AP} and R_P represent the parallel and anti-parallel resistance of an MTJ, respectively. The pinned FM layer acts as a spin filter, thus, producing a higher density of majority spin-polarized electrons. The spin-polarized electrons will sustain their spin polarization while crossing the tunnel barrier to finally exert STT on the free layer and decide its final state.

For P to AP switching, current flows from SL to BL (see Fig. 2.2a) during which electrons flowing through the tunnel barrier are polarized in the direction of free layer. On reaching the pinned layer, the electrons with spins in the direction of pinned layer pass through, while others are reflected back to the free layer. These reflected electrons exert STT on the free layer to decide its eventual magnetization state. Since these reflected electrons are fewer in number, MTJ shows an asymmetric behavior such that the threshold switching current density for P to AP switching is larger than AP to P change. Moreover, during P to AP switching, the NMOS operates in source follower mode such that the gate to source voltage (V_{GS}) is less than the supply voltage (V_{DD}). Low V_{GS} reduces the drive current which is also known as source degeneration [9].

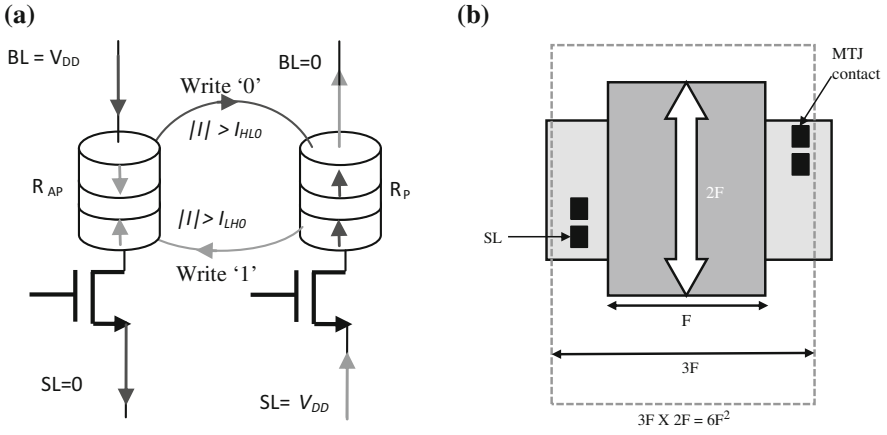

Fig. 2.2 **a** MTJ switching in STT MRAMs. **b** Layout of STT MRAM cell

Further, the Fig. 2.2b shows the layout of a typical 1T-1MTJ STT MRAM cell with a cell size of $6F^2$. The size of the cell depends on the minimum switching threshold current and current drivability of NMOS transistor. The major challenges associated with STT-MRAMs are: first, switching current reduction is crucial for achieving both high memory density and reducing the overall power consumption, second, sustaining high thermal stability for long period data retention [5].

2.2 Cell Size in Memories

The area required to store a single bit is known as cell size in memories. A comparison between different memory technologies is presented in Table 2.1 in terms of cell size [10]. The hard disk drives (HDDs) have the minimum cell size or highest integration density. Conventionally, the select device dominates the overall area occupied by a cell in most memory technologies [1]. International technology roadmap for semiconductors (ITRS) 2011 guidelines on memory design suggest a two terminal or vertical switch is the solution to growing needs of on-chip cache memory [1]. Researchers have proposed $6F^2$ cell with planar select devices and $4F^2$ cell with vertical select devices for various volatile and non-volatile memory technologies [2–4]. $4F^2$ cell on vertical silicon nano-wire (NW) platform has been demonstrated in various memory technologies. The $4F^2$ 1T-1R RRAM cell has been fabricated on vertical silicon NW platform by [4, 11–13]; wherein, the resistive random access memory (RRAM) stack is patterned to the same feature size above vertical GAA NW select device. 3D NAND flash memory of cell size $4F^2$ and beyond has been demonstrated by Kwong et al. [14]. Kawahara et al. [5] analyzed memory cell scalability for STT MRAMs for various transistor gate widths and informed the possibility of cell area reduction down to $4F^2$ with a vertical select device. However, no thorough analysis has been presented for vertical select device driving STT MRAM cells. Hence, experiments need to be initiated for realizing $4F^2$ architecture in the field of STT MRAMs too.

2.3 Next Generation $4F^2$ STT MRAM

The proposal for STT MRAM on a vertical silicon NW platform leads to the smallest cell area of $4F^2$. In logic applications with GAA devices, the source and gate contacts need to be created for each device. However, in the case of memory

Table 2.1 Comparison of cell size in different memory technologies

Technology	DRAM	SRAM	NAND flash	Hard disk drives	RRAM	STT MRAM
Cell size in (F^2)	6–12	140	1–4	2/3	4	20–60

applications, the source and gate terminals can be interconnected underneath. Here, the contacts need to be created after each data word. Thus, the proposed STT MRAM architecture with buried source line and word line saved significant area. Being circular in shape, the PMA MTJs can be stacked above the select device to save area. The planar MOSFETs have a saturation drive current per unit width of 900 μA/μm for high performance logic [15]. On the other hand, GAA MOSFETs have been reported to have a much higher saturation drive current of 2.6–2.9 mA/μm per unit diameter [16]. Hence, GAA transistor with the same diameter should provide a larger drive current. A vertical GAA transistor can act as an ideal select device that can provide sufficient drive current for efficient switching of an MTJ.

2.3.1 *Proposed Architecture*

The proposed architecture consists of a PMA MTJ stacked above the vertical GAA NMOS transistor is shown in Fig. 2.3. The diameter of the MTJ stack and silicon NW is F. The overall area of each cell is $4F^2$ as shown in Fig. 2.3. It has a buried n or n+ layer above the oxide (SiO_2) or p-Si substrate, which can be formed after the formation of p-type NW. This forms the buried source line (SL). The SL and word line (WL) contacts are brought out through vias. The structure of the vertical GAA NMOS is shown in Fig. 2.3b. For SL = V_{DD} and bit line (BL) = 0 condition, the vertical GAA transistor will be operating with the bottom-as-drain and top-as-source. Conversely, for BL = V_{DD} and SL = 0, the GAA transistor operates with top-as-drain and bottom-as-source (see Fig. 2.3a).

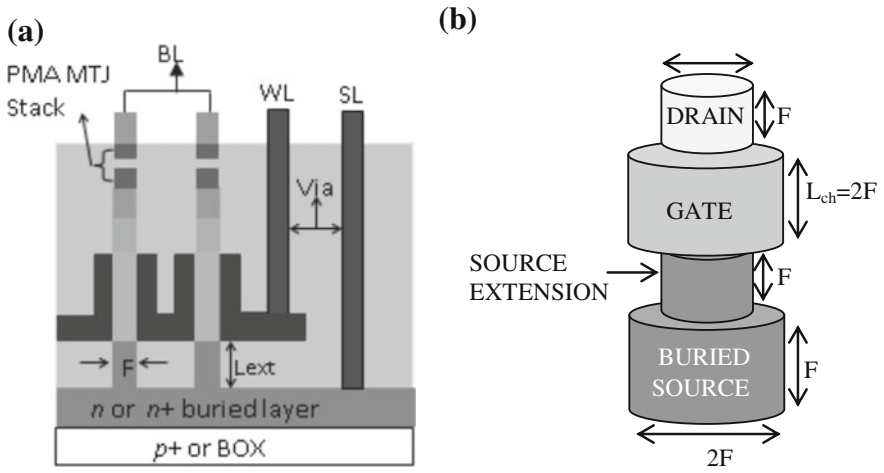

Fig. 2.3 **a** The architecture of vertical silicon NW 3D STT MRAMs. **b** The structure of vertical GAA NMOS select device

2.3.2 Performance Parameters and Windows

The performance parameters of STT MRAM can be well understood from Fig. 2.4 that demonstrates hysteretic behavior, cell current, and read/write windows. STT MARM write (read) operation is characterized by a write (read) margin and write (read) error rate. The write margins are defined as the difference between the write current and the switching threshold current [17]. Write error rate (WER) is the probability of failure during a particular write operation.

Read disturb rate (RDR) is the probability of accidental write during a read operation. Both, WER and RDR are quantified using the ubiquitous formalism of stochastic STT switching of a nano-magnetic layer at a finite temperature [18]. The probability of switching at a particular current ($I_{\text{write/read}}$), whether read or write, is expressed as,

$$P_{SW} = 1 - \exp\left\{-\frac{t_{PW}}{\tau_0}\exp\left[-\frac{E}{k_B T}\left(1 - \frac{I_{write/read}}{I_{C0}}\right)\right]\right\} \tag{2.1}$$

where, t_{PW} is the pulse width of read/write current, τ_0 is the inverse of the attempt frequency, I_{C0} is the switching threshold current (either I_{LH0} or I_{HL0}), $E/k_{\text{B}}T$ is the thermal stability factor for an MTJ. Using this expression, the WER and RDR are expressed as

$$WER = 1 - P_{SW}, RDR = P_{SW} \tag{2.2}$$

WER decreases with an increase in write current above the threshold current. For reliable write (read) operation in STT MRAM, WER (RDR) should be less than

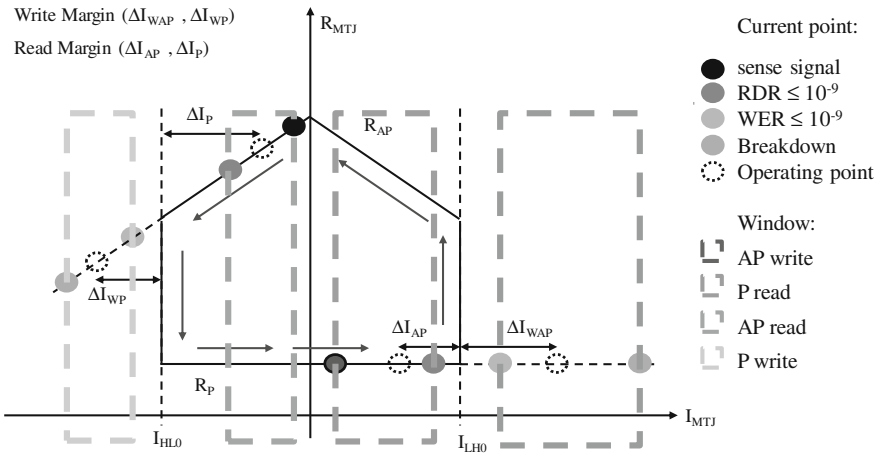

Fig. 2.4 Demonstrating resistance current hysteresis loop with read and write window

10^{-9} and thus sets the minimum (maximum) allowed value of write (read) current. The upper limit on write current is set by thin dielectric layer's breakdown voltage.

In conventional STT MRAM cells, the supply voltage (V_{DD}) is constant at a particular technology node. The minimum cell size in STT MRAM is determined by the smaller of the two write margins WM_P and WM_{AP}. The width of the access device is increased to achieve an appropriate value of overall WM. However, in order to maintain the overall area of GAA based STT MRAM cell to $4F^2$, the diameter of nano-wire has been kept constant. In addition, the vertical nano-wire technology does not allow the same flexibility of changing the dimensions as the conventional CMOS technology. Therefore, it is more suitable that the supply voltage V_{DD} is varied to achieve the optimum write current in vertical NW based STT MRAM.

2.3.3 Simulation Framework

Till date, STT MRAMs have been realized using planar CMOS technology only. The minimum attainable single cell size with a planar *n*-channel metal oxide semiconductor (NMOS) as access/select device is 6–$8F^2$. Using vertical NMOS as a select device, the cell area can be reduced to $4F^2$ [1, 5]. Since, calibrated SPICE models are not available for such novel structured devices; therefore, their impact on MRAMs cannot be analyzed on SPICE. It is advisable to use mixed mode device-circuit simulation framework shown in Fig. 2.5 to understand the effect of device design on MRAMs and non-volatile hybrid MTJ based logic circuits. TCAD device simulator is used to obtain the performance of an arbitrary select device such

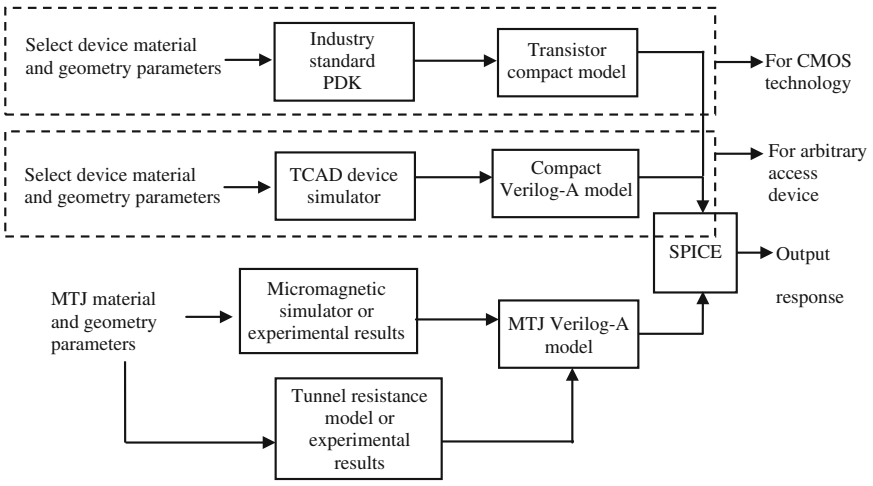

Fig. 2.5 SPICE based mixed mode simulation framework with Verilog-A MTJ model

as a vertical GAA transistor. Here, a micromagnetic simulator can also be used for calculating threshold switching current for an MTJ [19]. The simulation platform used is decided by a tradeoff between computation time and accuracy.

2.4 Case Study

In this section, using a case study the performance of STT MRAM with vertical select devices is analyzed. A comparison with conventional planar STT MRAM cell is also presented. The proposed STT MRAM cell is analyzed using calibrated Verilog-A models for PMA MTJ and vertical GAA NMOS transistor (BSIM CG) by HSPICE simulations. Write/dynamic power dissipation will be same for both vertical GAA and planar STT MRAM cells while using SiO_2 gate dielectric (GD) based select device. Hence, in the second part of the case study a superior 3-dimensional (3D) vertical silicon nano-wire (NW)/GAA with high-k (HfO_2) gate dielectric device based STT MRAM is presented. A significant improvement in write power can be achieved using high-k gate GAA device, as it provides higher drive current capability at lower supply voltage (V_{DD}). In addition, the implementation of high-k gate dielectric does not have any explicit impact on the MTJ switching time; and hence, does not affect the delay performance in STT MRAMs and MTJ based hybrid spintronic-CMOS circuits. In contrast to this, the conventional CMOS circuits follow the standard inverse relationship between delay and drive current, wherein, the propagation delay decreases continuously with an increase in drive current [20]. Using high-k GDs in CMOS circuits, the increased gate capacitive delay annuls the effect of increase in the drive current. In STT MRAMs, an inherent MTJ magnetization switching delay of 0.1–1 ns is inevitably present for all practical write current densities [21]. Hence, the high-k devices can be used to improve power savings as long as the increase in delay is small compared to MTJ switching delay. The proposed STT MRAM cell with high-k select device can achieve an appreciably larger tradeoff window between power dissipation and write margin (WM) while retaining appreciably good delay performance.

2.4.1 TCAD Analysis

In this section, the proposed select device structure is analyzed using TCAD device simulator. The analysis has been carried out for F = 40 nm, which is same as the diameter of the MTJ to keep the overall cell area $4F^2$. The proposed structure with a buried source of diameter $2F$ is shown in Fig. 2.6. The source is extended upwards to a height of F = 40 nm so that the gate and source are not shorted together. The diameter of the extension region is also F (40 nm). The drain is at the top having a diameter and length of F (40 nm). Device simulations are carried out for the

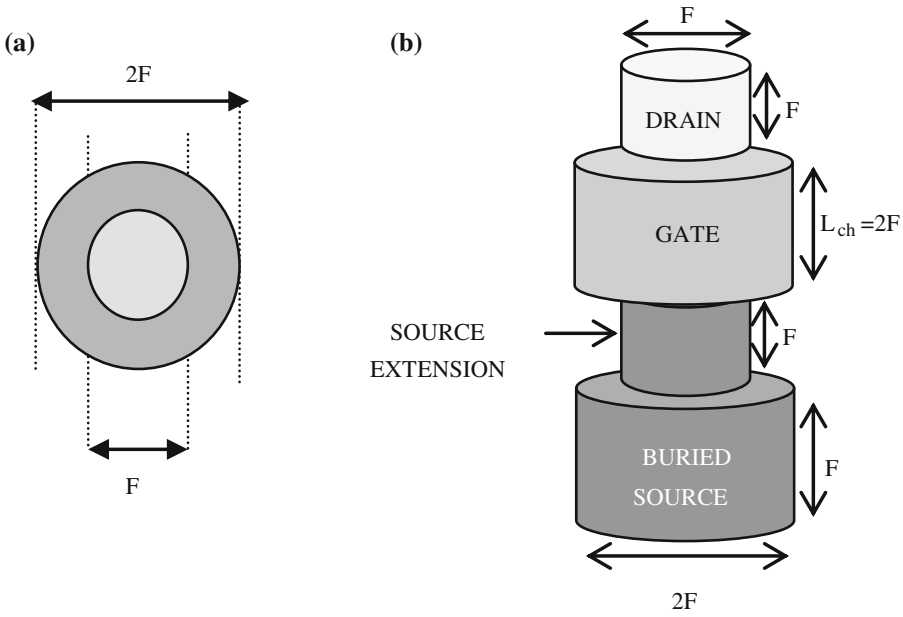

Fig. 2.6 **a** Top view **b** front view of the vertical GAA NMOS device

proposed GAA structure on TCAD [22] for gate/channel lengths (L_{ch}) of 40 (F), 80 ($2F$), and 120 nm ($3F$). The buried substrate layer is not shown for simplicity.

Source, drain, and source extension regions are heavily doped with a uniform n-type doping concentration of 1×10^{20} cm^{-3}. The channel is uniformly doped with a p-type doping concentration of 1×10^{16} cm^{-3}. The work function and gate oxide thickness of the cylindrical gate are 4.61 eV and 2 nm, respectively. The heavily doped extension region ensures a high current drive. The gate dielectric and feature size used during simulations are mentioned, specifically, when changed for the select devices.

2.4.2 TCAD Simulation Setup

TCAD device simulator self-consistently solves the Poisson and carrier continuity equations. Fermi-Dirac and band-gap narrowing based carrier statistics model are activated to account for carrier transport with heavily doped source/drain regions. Besides this, the Lombardi CVT (concentration, voltage, temperature) mobility model is used to accounts for all common effects related to carrier mobility in non-planar devices. The dependence of carrier mobility on impurity concentration, transverse electric field, longitudinal electric field, velocity saturation, and temperature are captured using the Lombardi's model. Furthermore, concentration-dependent Shockley-Read-Hall (SRH) recombination/generation model is also included in the TCAD simulation setup.

2.4.3 Mixed-Mode Simulation Results

The I_D-V_{DS} and I_D-V_{GS} characteristics obtained from TCAD device simulation are used to calculate threshold voltage, drain induced barrier lowering (*DIBL*), subthreshold slope (SS), and I_{ON}/I_{OFF} for L_{ch} of 40, 80, and 120 nm (F = 40 nm for SiO_2 gate dielectric devices). The method used for threshold voltage extraction is "the linear extrapolation method in the linear region" which is commonly known as "maximum transconductance method" [23, 24]. The magnitude of ON current (I_{ON}) and OFF current (I_{OFF}) are calculated at $V_{GS} = V_{DS} = 1.6$ V and $V_{GS} = 0$, $V_{DS} = 1.6$ V, respectively. *DIBL* is defined as the normalized difference in threshold voltages when V_{DS} is changed from V_{DS_lin} to V_{DS_sat}.

$$DIBL = (V_{t\_lin} - V_{t\_sat})/(V_{DS\_sat} - V_{DS\_lin}) \tag{2.3}$$

where, V_{t_lin} and V_{t_sat} are the threshold voltage in the linear (very low V_{DS}) and saturation region, respectively. The values of V_{DS_sat} and V_{DS_lin} are 1.6 V and 0.05 V, respectively. V_{t_sat} is the value of V_{GS} on I_D-V_{GS} curve for $V_{DS} = V_{DS\_sat}$ required to get the same value of current, which is obtained when $V_{GS} = V_{t\_lin}$ and $V_{DS} = V_{DS\_lin}$. The subthreshold slope (*SS*) is the change in V_{GS} required for altering the subthreshold drain current by one decade (10 times). The corresponding results are shown in Table 2.2. Although, the device with 40 nm gate length has the largest current drive, but it severely suffers from short channel effects. The *DIBL*, OFF current, and subthreshold slope parameters are comparatively large for the device with 40 nm gate length. It is because of lower electrostatic gate control at smaller gate length. Evidently, the device with 120 nm gate length demonstrates the best performance. The smaller gate length would also mean higher Joule heating in a smaller volume. Hence, larger gate length should be preferred for the vertical GAA architecture in STT MRAM.

In order to compare the performance of GAA based cell with the conventional STT MRAM cell, TCAD simulations are carried out for planar NMOS transistor also. The gate work function and oxide thickness of the planar NMOS are 4.61 eV and 1.5 nm, respectively. However, the source, drain, and channel doping are same as that for GAA NMOS. The performance parameters calculated for a planar NMOS with different device dimensions are placed in Table 2.3. The performance of the planar NMOS is poor, especially for small gate-length, due to large short channel effects that are measured at a high V_{DD} of 1.6 V. Although, the short channel effects of the planar NMOS can be reduced by decreasing the source and

Table 2.2 TCAD results of SiO_2 GD GAA device for different gate lengths

L_{ch} (nm)	V_{t_lin} (V)	DIBL (mV/V)	I_{ON} (μA)	I_{ON}/I_{OFF}	*SS* (mV/decade)
40	0.279	115.0	214.6	3.8×10^3	103.0
80	0.300	22.1	194.0	3.3×10^6	63.4
120	0.307	13.6	175.5	1.5×10^7	60.3

Table 2.3 TCAD results of planar NMOS device with SiO_2 GD

W_{NMOS} (nm)	L_{ch} (nm)	V_{t_lin} (V)	$DIBL$ (mV/V)	I_{ON} (μA)	I_{ON}/I_{OFF}	SS (mV/decade)
40	80	0.250	354.0	85.8	18.3	768.3
40	120	0.275	280.0	72.8	142.8	294.2
80	120	0.275	310.0	145.6	142.7	294.2

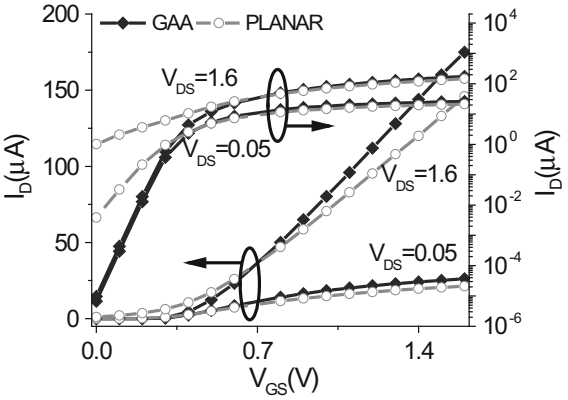

Fig. 2.7 Comparison of the I_D-V_{GS} characteristics of GAA (40 nm nano-wire diameter and L_{ch} = 120 nm) and planar (W_{NMOS} = 80 nm and L_{ch} = 120 nm) NMOS with SiO_2 GD

drain doping concentration, but that will reduce I_{ON} also. A comparison of I_D-V_{GS} characteristic in Fig. 2.7 confirms that GAA NMOS has much lower OFF current than the planar NMOS devices.

For SL = V_{DD} and BL = 0, the vertical GAA transistor would be operating with the bottom-as-drain and top-as-source. Therefore, the I_D-V_{DS} characteristics of the proposed structure should also be analyzed with the bottom-as-drain (buried source in Fig. 2.6). However, Fig. 2.8 clearly shows a minute difference between $|I_D|$-$|V_{DS}|$

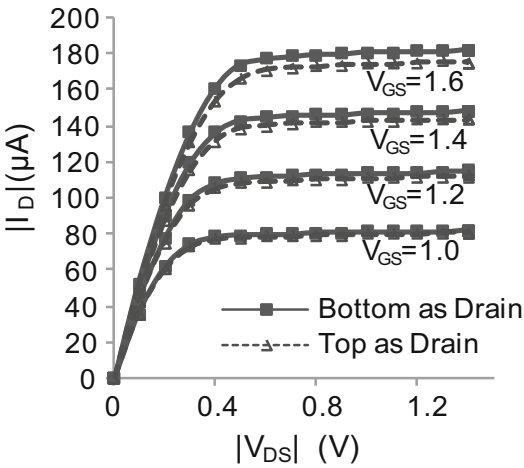

Fig. 2.8 Comparison of $|I_D|$-$|V_{DS}|$ characteristics with top-as-drain and bottom-as-drain operation for the GAA NMOS of 40 nm diameter (SiO_2 GD) with L_{ch} = 120 nm

Table 2.4 Comparison between proposed cell and $10F^2$ cell with planar NMOS (at V_{DD} = 1.6 V, F = 40 nm and SiO_2 GD)

Select device	WM_P (μA)	WM_{AP} (μA)	t_p (ns)	t_{AP} (ns)	Power (pW) WL = 0 V	Power (μW) WL = 1.6 V
GAA	23.3	34.0	0.43	0.25	16.2	112.4
Planar	17.6	29.0	0.52	0.32	1140.0	107.0

characteristics under the two modes of operation. This difference can be safely neglected in the subsequent analysis and the device can be considered to be having symmetric *I-V* characteristics.

The proposed STT MRAM cell and conventional cell with planar NMOS are analyzed using transient simulations on HSPICE using calibrated Verilog-A models. The results are placed in Table 2.4. Undoubtedly, the proposed cell demonstrates a better performance in terms of power dissipation and WMs. The leakage power dissipation for the proposed cell is 3 orders of magnitude lower than the conventional cell (when the cell is not selected for writing). The dynamic power dissipation at WL = 1.6 V (V_{DD}) is higher, although, here, the point of consideration is that the dynamic power always has a tradeoff with the P and AP WMs (write currents). There is a larger tradeoff window between the WM and dynamic power dissipation in the case of proposed cell with GAA device. The operation of proposed GAA based cell is also shown in Fig. 2.9 using a timing diagram.

2.4.4 *Impact of High-*k *GAA Devices*

Till now, the STT MRAM cells with vertical GAA device use SiO_2 GD. However, to fully explore the impact of all around gate control of vertical GAA devices on STT MRAM cells, HfO_2 based devices with high dielectric constant of 22 need to be used. In this section, the impact of high-k (HfO_2) GAA select device on the performance of an STT MRAM cell is analyzed. In addition, its performance is compared to STT MRAM cell using GAA devices with the conventional SiO_2 gate dielectric. Initially, TCAD simulations are carried out from feature size of 40–70 nm, while taking into account the mobility degradation effect in high-k (HfO_2) GD devices [25]. The mobility degradation is benchmarked using data obtained from Chau et al. [26] for metal gate devices. The work function and gate dielectric thickness are considered as 4.61 eV and 2 nm, respectively. Compact Verilog-A models are developed and calibrated individually for the HfO_2 GD based vertical GAA transistor and PMA MTJ.

Berkeley short-channel IGFET (Insulated gate field effect transistor) model of combined multi-gate (BSIM CMG) [27] is calibrated based on the results acquired from TCAD device simulations. Moreover, experimental results [28, 29] for high-performance PMA MTJs from Table 2.5 are used to calibrate compact

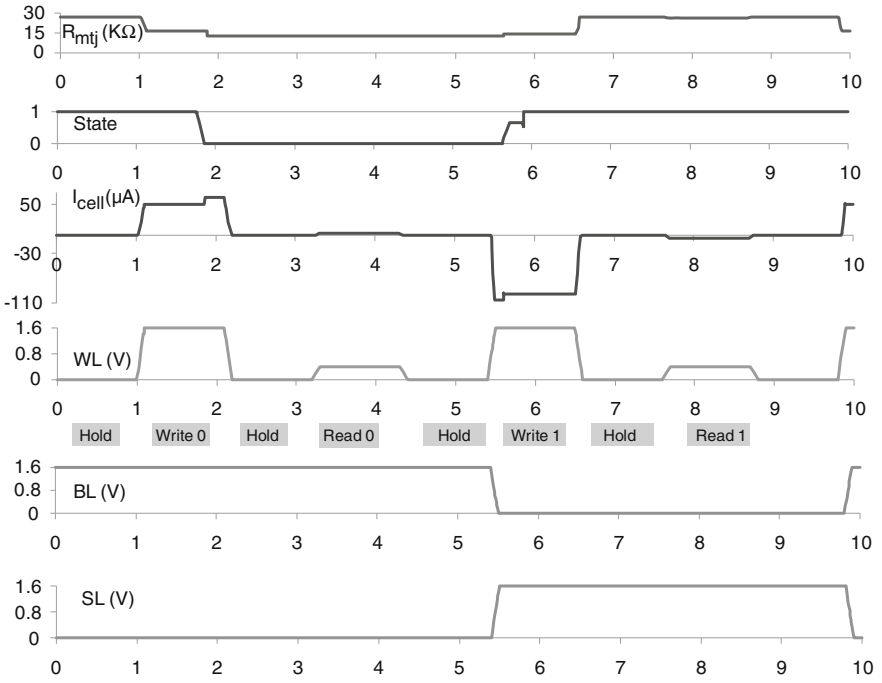

Fig. 2.9 A timing diagram showing the successful operation of the proposed $4F^2$ STT MRAM cell at V_{DD} = 1.6 V

Table 2.5 Experimental results for PMA MTJs

MTJ stack	Diameter (F in nm)	*TMR* (%)	*RA* (Ω-μm^2)	STT efficiency (k_BT/μA)
stack-1 [28]	40–70	102	6.6	1.3–3.0
stack-2 [29]	30–70	150	12	2.2–3.8

*STT efficiency is the ratio of $\Delta = E/k_BT$ in units of k_BT and I_{C0}, where I_{C0} is the average of (I_{LH0} and I_{HL0}) and Δ is the Boltzmann's stability factor. *RA* and *TMR* are the resistance area product and tunnel magneto-resistance of an MTJ, respectively.

Verilog-A models corresponding to low *RA* stack-1 and high *RA* stack-2. Here, STT efficiency is the ratio of Δ (= E/k_BT in units of k_BT) and I_{C0}, where, I_{C0} is the average of (I_{LH0} and I_{HL0}), and Δ is the Boltzmann's/thermal stability factor.

Bit cell level HSPICE simulations are carried out using calibrated compact models at different values of V_{DD} and F. The pulse width of write current lies between 2 and 50 ns so as to provide sufficient time for switching at given F. The write currents and threshold switching currents (I_{LH0} and I_{HL0}) for different feature sizes ranging from 40 to 70 nm are shown in Fig. 2.10a, b when SYM HfO_2 and SiO_2 based GAA devices are used in STT MRAM cells. It is clearly observed that

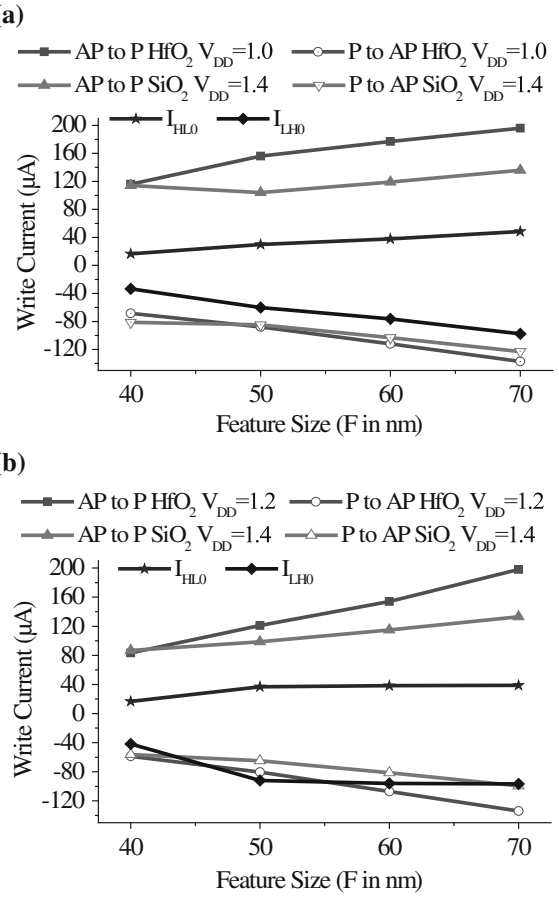

Fig. 2.10 Comparison between the write current obtained for STT MRAM cells with high-*k* (HfO_2) and SiO_2 GD vertical GAA NMOS devices **a** low *RA* MTJ stack-1 used during simulation **b** high *RA* stack-2 used during simulation

for all *F* between 40 and 70 nm, the high-*k* devices can be employed to achieve high WMs at lower V_{DD} (by 0.4 V). Although the write current for P to AP switching are overlapping for SiO_2 and high-*k* cells, but the analysis of SiO_2 cells was carried out at a higher V_{DD} of 1.4 V. Hence, high-*k* devices can reduce power dissipation in STT MRAMs by V_{DD} reduction.

2.4.5 *Impact of High-*k *GD on Delay*

The additional delay introduced due to the use of select devices with high-*k* gate dielectric is compared with the switching time of MTJ. The introduction of the high-*k* dielectric increases the WL capacitance. Elmore delay model [20] is used to determine the delay from the write line driver node to the gate electrode of a

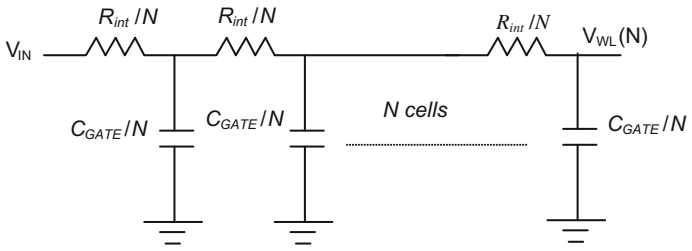

Fig. 2.11 Equivalent RC model for the 3D NW STT MRAM architecture

particular select device. If C_{GATE}/N is the gate capacitance and R_{int}/N is the interconnect resistance between cells (see Fig. 2.11), the propagation delay (τ_D) at WL after N cells is expressed as,

$$\tau_D = R_{\text{int}} C_{GATE} \left(\frac{N+1}{N} \right) \tag{2.4}$$

The propagation delay of N (N = 100 and 200) cells for different gate dielectrics is compared with the typical switching time of PMA MTJ at current of 100 μA. The percentage WL delay normalized by the MTJ switching time is plotted in Fig. 2.12. For N = 100 cells the delay of HfO_2, SiO_2 and Si_3N_4 is less than 10% of the switching time required by a PMA MTJ. Hence, high-k gate dielectric select devices need to be analyzed thoroughly, because they could lead to V_{DD} reduction at the cost of increase in WL capacitance. As, this delay due to the increase in WL capacitance can be considered nominal with respect to MTJ switching time.

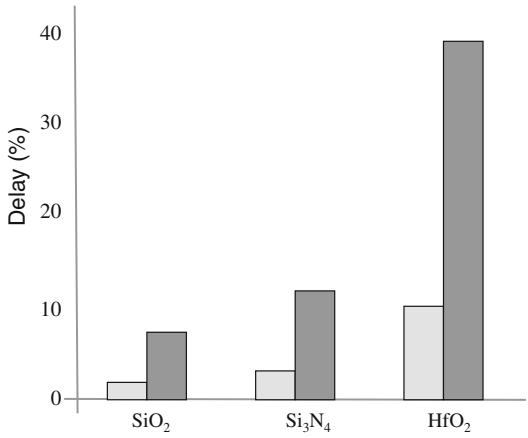

Fig. 2.12 Percentage switching delay of WL after N cells for various dielectrics with respect to MTJ switching delay

2.5 Proposed Fabrication Methodology

Several research groups have successfully fabricated $4F^2$ cell with vertical select devices for various memory technologies [11, 12, 14] on vertical silicon nano-wire platform. The 1T-1-resistor resistive random access memory (RRAM) cell has been fabricated on vertical silicon nano-wire (NW) platform by [4, 11–13] wherein the RRAM stack is patterned to the same feature size above vertical GAA NW select device. $4F^2$ 3D NAND flash and junction-less silicon-oxide-nitride-oxide-silicon (JL-SONOS) memory have been demonstrated in Kwong et al. [14]. Based on the methodology given in the aforementioned references, processing steps for fabricating $4F^2$ STT MRAM cell on vertical silicon NW platform are presented in Figs. 2.13 and 2.14.

The fabrication of MTJs should follow the same back-end-of-line (BEOL) semiconductor processing (see Fig. 2.13); wherein, the MTJ stack is deposited between successive metal interconnect layers after the front-end-of-line (FEOL) processing of the vertical GAA select device.

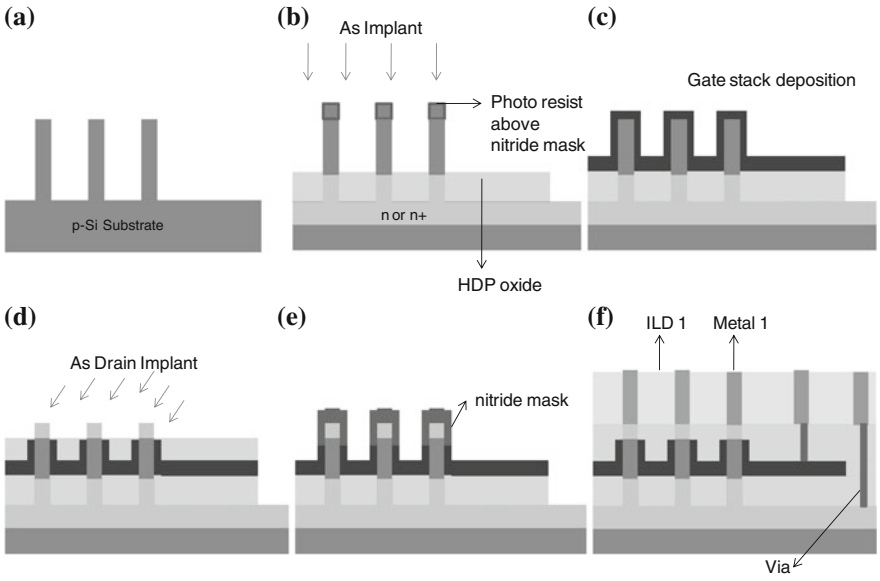

Fig. 2.13 FEOL Processing [13, 30, 31] **a** vertical pillar etch. **b** As implantation to form the source and source extension regions, high density plasma oxide deposition **c** gate stack deposition **d** top amorphous Si etched to expose drain and As drain implantation **e** nitride mask formation to prevent nano-pillar tip **f** high density plasma oxide deposition, chemical mechanical planarization for exposing and removing nitride mask, pre-metal dielectric oxide deposition, metallization with Al pads

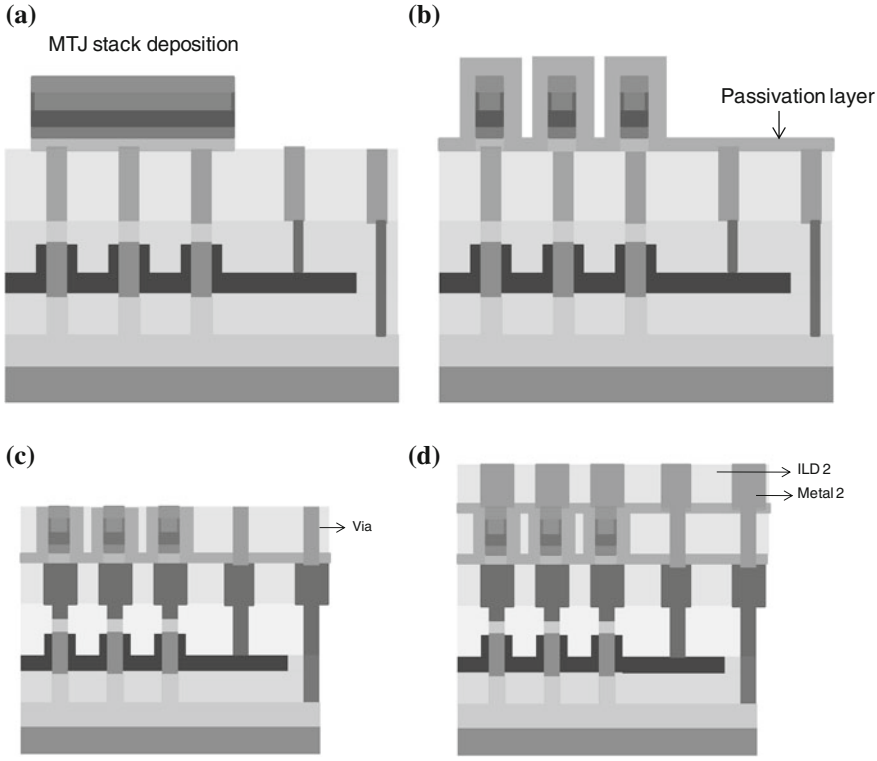

Fig. 2.14 BEOL Processing [32] **a** formation of MTJ stack over planarized surface. The stack includes first electrode (generally Ta), a fixed layer, tunnel barrier, free layer and second electrode. The fixed and free layers are generally composed of 2–3 layers. **b** A single mask etching process and deposition of dielectric passivation layer for protection. **c** ILD-1 deposition that encapsulates MTJ stack followed by removal using planarization, and via formation. **d** Another dielectric passivation, ILD2 deposition, planarization to expose, and metallization to form metal-2 interconnect

The fabrication of MRAMs involves multiple steps of deposition and etching during the fabrication of MTJ stack. Especially during the etching of primary layers (ferromagnetic layers and tunnel barrier) constituting an MTJ, the sidewall redeposition of unwanted material on MTJs could cause failure of the device [33, 34] The etching process should be highly selective which is difficult to achieve at low dimensions and further difficulties arise because of the vertical GAA NW transistor. The two major challenges during fabrication of STT MRAM cell are:

- The etching process that goes from the top electrode to bottom electrode should have a high selectivity so that the MTJ cell is protected from any erosion during etching. Retaining the parameters like *TMR* and stability factor is of paramount importance during etching and pattering of MTJ stack.

- The redeposition material should be completely removed by the end of etching cycle as it can cause shorts across the tunnel barrier of MTJ.

2.6 Conclusion

This chapter presented and analyzed the next generation 3D vertical silicon NW based STT MRAMs with vertical GAA select device. The design tradeoffs and constraints are analyzed taking into account the recently available PMA MTJs. Using a case study the performance of STT MRAM cell using vertical GAA select device is analyzed and compared with conventional STT MRAM with planar select device. The high driving capability provided a clear advantage over conventional planar access device which was reflected in simulation results presented in this chapter. TCAD simulations proved that the GAA device provided a drive current of 2.8 mA/μm as opposed to 1.16 mA/μm by planar access device at V_{DD} = 1.2 V (SiO_2 GD). Thus the proposed vertical silicon NW STT MRAMs offer excellent performance in terms of write margins, power dissipation while achieving maximum 2D array density of $4F^2$. Moreover, the analysis for feature size 70 nm demonstrates that the use of high-k device can reduce V_{DD} by 0.4 V, thereby, reducing write power up to 25%.

Problems

Multiple Choice

1. **The main bottleneck for the scalability of STT-MRAM array is**

   a. Pinned layer
   b. Free layer
   c. Tunnel barrier
   d. Select device

2. **One of the ferromagnetic layers of the MTJ is pinned using the material with**

   a. Low coercivity
   b. High coercivity
   c. Low retaintivity
   d. High retaintivity

3. **The write margin (*WM*) increases with the**

   a. Increase in switching threshold
   b. Decrease in operating current
   c. Increase in operating current
   d. None of these

4. **The read disturb rate (*RDR*) decreases with**

   a. Decrease in switching threshold
   b. Increase in read current
   c. Increase in thermal stability factor
   d. All of these

5. **The overall delay of high-*k* GD based GAA device**

   a. Remains constant
   b. Decreases
   c. Increases
   d. None of these

6. **The purpose of source extension region is**

   a. To keep separate gate and buried source
   b. To make shorted gate and buried source
   c. To increase the source length
   d. To enhance the performance

7. **The overall delay of STT-MRAM using high-*k* GD based GAA device**

   a. Increases
   b. Remains constant
   c. Decreases
   d. None of these

8. **For an MTJ, Read disturb rate (RDR) is**

   a. The probability of false read operation during a write operation
   b. The probability of no write during read operation
   c. The probability of accidental write during a read operation
   d. None of the above

9. **For an MTJ, the width of the access device is increased to**

   a. Achieve an appropriate value of overall write margin
   b. To reduce the overall write margin
   c. To reduce the write error rate
   d. To reduce the heating effect

10. **The high-*k* gate GAA improves the write power due to**

    a. Low drive current at high voltage
    b. High drive current capability at low voltage
    c. High drive current at high voltage
    d. None of the above

Answer Keys: 1-d, 2-b, 3-c, 4-d, 5-c, 6-a, 7-b, 8-c, 9-a, 10-b

Short Answers

1. Explain the advantages of STT-MRAM for making it strong contender for futuristic embedded memory technology.
2. Describe the tunnel barrier reliability issues.
3. Enlist the advantages of high-*k* devices.
4. Analyze the experimental results for PMA MTJs.
5. Enlist the steps for FEOL processing.

References

1. Emerging research devices (2011). *International technology road map for semiconductors* [Online]. Available: http://www.itrs.net
2. T. Schloesser, F. Jakubowski, J. V. Kluge, A. Graham, S. Slesazeck, M. Popp, P. Baars, K. Muemmler, P. Moll, K. Wilson, A. Buerke, D. Koehler, J. Radecker, E. Erben, U. Zimmermann, T. Vorrath, B. Fischer, G. Aichmayr, R. Agaiby, W. Pamler, T. Schuster, W. Bergner, and W. Mueller, "$6F^2$ buried wordline DRAM cell for 40 nm and beyond," *Proc. IEEE Int. Elect. Dev. Meet.* (*IEDM 2008*), San Francisco, CA, 2008, pp. 1–4.
3. H. Chung, H. Kim, H. Kim, K. Kim, S. Kim, K.-W. Song, J. Kim, Y. C. Oh, Y. Hwang, H. Hong, G.-Y. Jin, and C. Chung, "Novel $4F^2$ DRAM cell with vertical pillar transistor (VPT)," *Proc. IEEE Eur. Sol. Dev. Res. Conf.* (*ESSDERC 2011*), Helsinki, 2011, pp. 211–214.
4. Z. Fang, X. P. Wang, X. Li, Z. X. Chen, A. Kamath, G. Q. Lo, and D. L. Kwong, "Fully CMOS-compatible 1T1R integration of vertical nanopillar GAA transistor and oxide-based RRAM cell for high-density," *IEEE Trans. Elect. Dev.,* vol. 60, no. 3, pp. 1108–1113, 2013.
5. T. Kawahara, K. Ito, R. Takemura, and H. Ohno, "Spin-transfer torque RAM technology: review and prospect," *Microelect. Reliab.*, vol. 52, no. 4, pp. 613–627, 2012.
6. S. Ikeda, H. Sato, M. Yamanouchi, H. Gan, K. Miura, K. Mizunuma, S. Kanai, S. Fukami, F. Matsukura, N. Kasai, and H. Ohno, "Recent progress of perpendicular anisotropy magnetic tunnel junctions for nonvolatile VLSI," *Spin World Sci.*, vol. 02, no. 03, pp. 1240003-1–1240003-12, 2012.
7. S. Ikeda, J. Hayakawa, Y. M. Lee, F. Matsukura, and Y. Ohno, T. Hanyu, H. Ohno "Magnetic tunnel junctions for spintronic memories and beyond," *IEEE Trans. Elect. Dev.*, vol. 54, no. 5, pp. 991–1002, 2007.
8. T. Kawahara, R. Takemura, K. Miura, J. Hayakawa, S. Ikeda, Y. M. Lee, R. Sasaki, Y. Goto, K. Ito, T. Meguro, F. Matsukura, H. Takahashi, H. Matsuoka, and H. Ohno, "2 Mb SPRAM (spin-transfer torque RAM) with bit-by-bit bi-directional current write," *IEEE Trans. Sol. Cir.*, vol. 43, no. 1, pp. 109–120, 2008.
9. S. Verma, P. K. Pal, S. Mahawar, and B. K. Kaushik, "Performance Enhancement of STT MRAM using asymmetric-*k* sidewall-spacer NMOS," *IEEE Trans. on Elect. Dev.*, vol. 63, no. 7, pp. 2771–2776, 2016.
10. J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing.," *Nat. Nanotech.*, vol. 8, no. 1, pp. 13–24, 2013.
11. X. P. Wang, Z. X. Chen, X. Li, A. R. Kamath, L. J. Tang, D. Mei, Y. Lai, P. C. Lim, D. Teng, H. Li, N. Singh, P. Guo, Q. Lo, and D. Kwong, "HfOx-based RRAM cells with fully CMOS compatible technology," *Proc. IEEE Int. Conf. Sol. Inte. Cir.* (*ICSIC 2012*), Singapore, 2012, pp. 1–6.

12. B. Chen, X. Wang, B. Gao, Z. Fang, J. Kang, L. Liu, X. Liu, G.-Q. Lo, and D.-L. Kwong, "Highly compact ($4F^2$) and well behaved nano-pillar transistor controlled resistive switching cell for neuromorphic system application," *Nat. Sci. Rep.*, vol. 4, pp. 6863-1–6863-5, 2014.
13. X. Wang, Z. Fang, X. Li, and B. Chen, "Highly compact 1T-1R architecture ($4F^2$ footprint) involving fully CMOS compatible vertical GAA nano-pillar transistors and oxide-based RRAM cells exhibiting excellent NVM properties and ultra-low power operation," *Proc. IEEE Int. Elect. Dev. Meet.* (*IEDM 2012*), San Francisco, CA, 2012, pp. 20.6.1–20.6.4.
14. D.-L. Kwong, X. Li, Y. Sun, G. Ramanathan, Z. X. Chen, S. M. Wong, Y. Li, N. S. Shen, K. Buddharaju, Y. H. Yu, S. J. Lee, N. Singh, and G. Q. Lo, "Vertical silicon nanowire platform for low power electronics and clean energy applications," *J. Nanotechn.*, vol. 2012, pp. 1–21, 2012.
15. Process integration device and structures (2001). *International technology roadmap for semiconductors* [Online]. Available: http://www.itrs.net
16. Y. Song, Q. Xu, J. Luo, and H. Zhou, "Performance breakthrough in gate-all-around nanowire n- and p-type MOSFETs fabricated on bulk silicon substrate," *IEEE Elect. Dev. Lett.*, vol. 59, no. 7, pp. 1885–1890, 2012.
17. S. Verma, S. Kaundal, and B. K. Kaushik, "Novel $4F^2$ buried-source-line STT MRAM cell with vertical GAA transistor as select device," *IEEE Trans. on Nanotechn.*, vol. 13, no. 6, pp. 1163–1171, 2014.
18. Z. Li and S. Zhang, "Thermally assisted magnetization reversal in the presence of a spin-transfer torque," *Phys. Rev. B*, vol. 69, no. 13, p. 134416, Apr. 2004.
19. S. Verma, M. S. Murthy, and B. K. Kaushik, "All spin logic (ASL): A micromagnetic perspective," *IEEE Trans. on Mag.*, vol. 51, no. 10, pp. 3400710-1–3400710-7, 2015.
20. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital integrated circuits: A design perspective, Upper Saddle River, NJ, Prentice-Hall, 2003, pp. 177–233.
21. D. D. Tang, and Y. J. Lee, Magnetic memory fundamentals and technology, Cambridge, UK, Cambridge University Press, 2010, pp. 122–164.
22. ATLAS user's manual, Silvaco Inc., 2012. Available: www.silvaco.com
23. L. Dobrescu, M. Petrov, D. Dobrescu, and C. Ravariu, "Threshold voltage extraction methods for MOS transistors," *Proc. 23rd IEEE Int. Semicond. Conf.* (*CAS 2000*), Sinaia, 2000, pp. 371–374.
24. A. Bazigos, M. Bucher, J. Assenmacher, S. Decker, W. Grabinski, and Y. Papananos, "An adjusted constant-current method to determine saturated and linear mode threshold voltage of MOSFETs*," IEEE Trans. Elect. Dev.*, vol. 58, no. 11, pp. 3751–3758, 2011.
25. W. J. Zhu, and T. P. Ma, "Temperature dependence of channel mobility in HfO_2-gated NMOSFETs," *IEEE Elect. Dev. Lett.*, vol. 25, no. 2, pp. 89–91, 2004.
26. R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, "Application of high-*k* gate dielectrics and metal gate electrodes to enable silicon and non-silicon logic nanotechnology," *Microelect. Eng.*, vol. 80, pp. 1–6, 2005.
27. V. Sriramkumar, N. Paydavosi, J. Duarte, D. Lu, C. Hsun Lin, M. Dunga, S. Yao, T. Morshed, A. Niknejad and C. Hu, "BSIM-CMG 107.0.0 multi-gate MOSFET compact model: technical manual," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, 2013.
28. G. Jan, Y.-J. Wang, T. Moriyama, Y.-J. Lee, M. Lin, T. Zhong, R.-Y. Tong, T. Torng and P.-K Wang "High spin torque efficiency of magnetic tunnel junctions with MgO/CoFeB/MgO free layer," *Appl. Phys. Exp.*, vol. 5, pp. 093008-1–093008-3, 2012.
29. L. Thomas, G. Jan, J. Zhu, H. Liu, Y.-J. Lee, S. Le, R.-Y. Tong, K. Pi, Y.-J. Wang, D. Shen, R. He, J. Haq, J. Teng, V. Lam, K. Huang, T. Zhong, T. Torng, and P.-K. Wang, "Perpendicular spin transfer torque magnetic random access memories with high spin torque efficiency and thermal stability for embedded applications (invited)," *J. Appl. Phys.*, vol. 115, no. 17, pp. 172615-1–172615-6, 2014.

30. B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong, "Vertical silicon-nanowire formation and gate-all-around MOSFET," *IEEE Elect. Dev. Lett.*, vol. 29, no. 7, pp. 791–794, 2008.
31. R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-nanowire *n*-type tunneling FETs with low subthreshold swing at room temperature,' *IEEE Elect. Dev. Lett.*, vol. 32, no. 4, 437–439, 2011.
32. S. H Kang, D. Bang, and K. Lee, "One-mask MTJ integration for STT MRAM," U.S. Patent 2009/0261433 A1, 2009.
33. E. J. O'Sullivan, Magnetic tunnel junction-based MRAM and related processing issues "*IBM Research Report*," RC23525, 2005.
34. Yuchen Zho, and Yiming Huai, "STT-MRAM manufacturing method with in-situ annealing," U.S. Patent US8758850 B2, June 24, 2014.

Springer

http://www.springer.com/978-981-10-2719-2

Next Generation Spin Torque Memories
Kaushik, B.K.; Verma, S.; Kulkarni, A.A.; Prajapati, S.
2017, XVII, 92 p. 64 illus., Softcover
ISBN: 978-981-10-2719-2