

Contents

1	Introduction to On-Chip Interconnects and Modeling	1
1.1	Introduction	1
1.2	Evolution of Interconnect Materials	2
1.2.1	Carbon Nanotubes (CNTs)	3
1.2.2	Graphene Nanoribbons (GNRs)	4
1.3	Modeling of On-Chip Interconnects	4
1.4	Introduction to FDTD Method	6
1.4.1	Central Difference Approximation	7
	References	8
2	Interconnect Modeling, CNT and GNR Structures, Properties, and Characteristics	11
2.1	Interconnect Modeling Approaches	11
2.1.1	Lumped Model with CMOS Driver	11
2.1.2	Distributed Model with Resistive Driver	12
2.1.3	Distributed Model with CMOS Driver	13
2.2	Carbon Nanotubes	14
2.2.1	Basic Structure of CNTs	14
2.2.2	Semiconducting and Metallic CNTs	18
2.2.3	Properties and Characteristics of CNTs	20
2.2.4	Conductivity Comparison	22
2.2.5	MWCNT Interconnect Modeling	24
2.2.6	MWCNT Performance Analysis	28
2.3	Graphene Nanoribbons	29
2.3.1	Basic Structure of GNRs	29
2.3.2	Semiconducting and Metallic GNRs	31
2.3.3	Properties and Characteristics of GNRs	31
2.3.4	Conductivity Comparison	33
2.3.5	MLGNR Interconnect Modeling	34
2.3.6	MLGNR Performance Analysis	36
	References	38

3	FDTD Model for Crosstalk Analysis of CMOS Gate-Driven Coupled Copper Interconnects	43
3.1	Introduction	43
3.2	Motivation	44
3.3	FDTD Model of CMOS Gate-Driven Cu Interconnects.	47
3.3.1	FDTD Model of Coupled Interconnects	48
3.3.2	Incorporation of Boundary Constraints	50
3.4	Validation of the Model	53
3.5	Extended Three Coupled Interconnect Lines	56
3.6	Summary	58
	References	59
4	FDTD Model for Crosstalk Analysis of Multiwall Carbon Nanotube (MWCNT) Interconnects	61
4.1	Introduction	61
4.2	Equivalent Single Conductor Model of the MWCNT Interconnect	63
4.2.1	Resistance	65
4.2.2	Inductance	65
4.2.3	Capacitance	67
4.3	FDTD Model of MWCNT Interconnect	68
4.3.1	The MWCNT Interconnect Line	68
4.3.2	Boundary Condition at Near-End Terminal	70
4.3.3	Boundary Condition at Far-End Terminal	71
4.4	Validation of the Model	72
4.5	Sensitivity Analysis	75
4.5.1	Sensitivity Analysis for Number of Conducting Channels	75
4.5.2	Sensitivity Analysis for Contact Resistance.	76
4.6	Summary	77
	References	77
5	Crosstalk Modeling with Width Dependent MFP in MLG NR Interconnects Using FDTD Technique.	81
5.1	Introduction	81
5.2	Equivalent Single Conductor Model of the MLG NR Interconnect	82
5.2.1	Transient Analysis of MTL and ESC Models	85
5.3	FDTD Model of the MLG NR Interconnect	86

- 5.4 Results and Discussion 89
 - 5.4.1 Analysis of Mean Free Path, Resistance, and Propagation Delay with Rough Edges 90
 - 5.4.2 Crosstalk-Induced Delay. 91
 - 5.4.3 Performance Comparison Between Cu and MLGNR Interconnects. 93
- 5.5 Summary 95
- References 95
- 6 An Efficient US-FDTD Model for Crosstalk Analysis of On-Chip Interconnects 97**
 - 6.1 Introduction 97
 - 6.2 Development of Proposed US-FDTD Model 98
 - 6.2.1 Modeling of Coupled On-Chip Interconnects 99
 - 6.2.2 Modeling of CMOS Driver. 101
 - 6.2.3 Modeling of Driver-Interconnect-Load 102
 - 6.2.4 Stability Analysis 106
 - 6.3 Simulation Setup and Results 107
 - 6.3.1 Transient Analysis. 108
 - 6.3.2 Crosstalk Induced Noise Peak, Width and Delay Analysis. 109
 - 6.3.3 Unconditional Stability of the Proposed Model 110
 - 6.3.4 Efficiency of the Proposed Model 111
 - 6.3.5 Comparison with 3D Simulations 112
 - 6.4 Performance Comparison of Cu, MWCNT and MLGNR Interconnects. 113
 - 6.5 Summary 115
 - References 115



<http://www.springer.com/978-981-10-0799-6>

Crosstalk in Modern On-Chip Interconnects

A FDTD Approach

Kaushik, B.K.; Kumar, V.R.; Patnaik, A.

2016, XV, 116 p. 71 illus., Softcover

ISBN: 978-981-10-0799-6