Preface

Advancement in VLSI technology offers gigascale integrated circuits in a system on-chip. In such circuits, interconnects play a key role in determining circuit performance such as time delay and power consumption. At high operating frequencies, the closely packed interconnects produce transient crosstalk. The crosstalk noise strongly influences the signal propagation delay and also causes logic or functional failure. Therefore, it is desirable to accurately model the crosstalk effects in the on-chip interconnects.

Over the years, several mathematical models have been proposed for the analysis of CMOS-gate-driven coupled interconnect lines. However, most of these crosstalk noise models consider the nonlinear CMOS driver as a linear resistor. This approximation is not valid for on-chip interconnects because during the input and output transition states the MOSFET operates in cutoff, linear, and saturation regions. The MOSFET operating time in the saturation region is about 50 % during the transition period. Moreover, the equivalent resistance value in saturation region is much higher than the linear region. Thus, assuming that the transistor operates in the linear region during the transition state leads to severe errors in the performance estimation of the driver interconnect load system. Therefore, it is necessary to develop an accurate model that appropriately considers the nonlinear effects of CMOS driver and accurately measures the crosstalk-induced performance parameters of on-chip interconnects. This book presents an accurate and time efficient model of CMOS-gate-driven coupled interconnects for crosstalk-induced performance analysis by considering the nonlinear effects of CMOS driver.

The conventional interconnect copper material suffers due to lower reliability with downscaling of interconnect dimensions. The reliability of Cu decreases due to electromigration-induced problems such as hillock and void formations. Moreover, with highly scaled dimensions the resistivity of copper increases due to electron-surface scattering and grain-boundary scattering. Therefore, researchers are forced to find an alternative material for on-chip interconnects. Carbon nanotubes (CNTs) have been proposed as a promising interconnect material. A portion of this book is focused toward modeling of MWCNT interconnects. Based on the electrical

equivalent model, an accurate FDTD model is presented while incorporating the quantum effects of nanowire and nonlinear effects of CMOS driver. The crosstalk noise is comprehensively analyzed by examining both functional and dynamic crosstalk effects.

Graphene nanoribbon (GNR), a strip of ultrathin width graphene layer, has also been considered aggressively by researchers as a potential alternative material for realizing on-chip interconnects. Most of the physical and electrical properties of GNRs are similar to that of CNTs; however, the major advantage of GNRs over CNTs is that both transistor and interconnect can be fabricated on the same continuous graphene layer, thus avoiding the metal-graphene contact problems. This book presents an accurate model for the analysis of MLGNR interconnects using the FDTD technique. In a more realistic manner, the model incorporates the width-dependent MFP parameter that helps in accurately estimating the crosstalk-induced performance in comparison to conventional models. Moreover, a comparative analysis of crosstalk-induced performance is presented among Cu, MWCNT, and MLGNR interconnects.

The stability of the FDTD technique is constrained by the Courant-Friedrichs-Lewy (CFL) stability condition. Hence, beyond the CFL condition, the technique is unstable and within it, the technique is inefficient. The efficiency improvements in the FDTD technique can be easily addressed if the CFL stability condition is removed by implicitly deriving the transmission line equations. To improve the efficiency of the FDTD technique, an unconditionally stable FDTD (US-FDTD) technique is presented for the analysis of MLGNR interconnects.

This book provides an accurate FDTD model for on-chip interconnects, covering most recent advancements in materials and design. Furthermore, depending on the geometry and physical configurations, different electrical equivalent models for CNT and GNR-based interconnects are presented. Based on the electrical equivalent models the performance comparison among the Cu, CNT, and GNR-based interconnects are also discussed. The proposed models are validated with the HSPICE simulations. The organization of the book is as follows: Chap. 1 introduces the current research scenario in modeling of on-chip interconnects. Chapter 2 presents the structure, properties, and characteristics of graphene based on-chip interconnects. The FDTD modeling of Cu-based on-chip interconnects is presented in Chap. 3. The model considers the nonlinear effects of CMOS driver as well as the transmission line effects of interconnect line that includes coupling capacitance and mutual inductance effects. Chapter 4 introduces an equivalent single conductor (ESC) model of MWCNT interconnects. Based on the ESC model, this chapter presents an accurate FDTD model of MWCNT while incorporating the quantum effects of nanowire and nonlinear effects of CMOS driver. The modeling of MLGNR interconnects using the FDTD technique is presented in Chap. 5. In a more realistic manner, the proposed model includes the effect of width-dependent MFP of the MLGNR while taking into account the edge roughness. Finally, to

improve the efficiency of the FDTD model, an unconditionally stable FDTD technique is presented for the analysis of on-chip interconnects in Chap. 6. Moreover, the performance of Cu interconnect is compared with MWCNT and MLGNR interconnects under the influence of crosstalk.

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