Chapter 2
Modulation for Power Electronic Converters

2.1 Introduction

At present, voltage source converters are mostly used in electrical drives. These converters utilize capacitors in the DC-link to store temporarily electrical energy. Switching the power electronic devices allows the DC voltage to be modulated which can result in a variable voltage and frequency waveform. The purpose of the modulator is to generate the required switching signals for these switching devices on the basis of user defined inputs. For this purpose, the voltage–time integral was introduced [68], which in turn is tied to the average voltage per sample \(U(t_k)\) that may be written as

\[
U(t_k) = \frac{1}{T_s} \int_{t_k}^{t_k+T_s} u(t) \, dt \tag{2.1}
\]

where \(T_s\) is a given sample interval and \(u(t)\) represents the instantaneous voltage across a single-phase of a load. The introduction of the variable \(T_s\) assumes the use of a fixed sampling frequency which is normally judiciously chosen higher than the fundamental frequency range required to control electrical machines. The upper sampling frequency limit is constrained by the need to limit the switching losses of the converter semiconductor devices.

The ability to control the converter devices in such a manner that the load is provided with a user defined mean reference voltage per sample \(U^*(t_k)\) is instrumental to control current accurately. This statement can be made plausible by considering the incremental flux linkage for one sample interval of a load in the form of a coil with inductance \(L\) and resistance \(R\) which may be written as

\[
\Delta \psi(t_k) = \int_{t_k}^{t_k+T_s} (u(t) - Ri(t)) \, dt \tag{2.2}
\]
The corresponding incremental change of load current (over a sample interval $T_s$) may be written as
\[ \Delta i(t_k) = \frac{\Delta \psi(t_k)}{L} \]
(2.3)
in the event that magnetic saturation effects may be ignored. This expression can, with the aid of (2.2), be expressed as
\[ \Delta i(t_k) = \frac{1}{L} \int_{t_k}^{t_k + T_s} u(t) \, dt - \frac{R}{L} \int_{t_k}^{t_k + T_s} i(t) \, dt \]
(2.4)
which may be reduced to
\[ \Delta i(t_k) \approx \frac{U(t_k) T_s}{L} \]
(2.5)
when the time constant $\tau = L/R$ of the load is deemed to be relatively large compared to $T_s$, as is normally the case for electrical machines. Central to the issue of controlling the incremental current is therefore, according to (2.5), the ability of the modulator to realize (within the constraint of this unit) the condition
\[ U(t_k) = U^*(t_k) \]
(2.6)
for each sampling instance. Note that (2.6) simply states that the switching states of the converter must be controlled by the modulator to ensure that the average voltage (per sample) equals the user defined average reference value to ensure that the actual and reference incremental current change (per sample interval) are equal.

How this may be achieved will be outlined in subsequent sections for various converter topologies using an approach taken by Svensson [63]. In effect, this approach considers how the average voltage per sample $U(t_k)$ varies as function of the converter switch on/off time within a sample interval. Once this relation is known for the converter under consideration, the function in question is compared with the user defined reference value to determine the converter switch state within each sample. Initially, a single-phase half-bridge converter, as discussed in [68], will be considered followed by an analysis of a single-phase full-bridge converter and three-phase converter. In the context of modulation for three-phase converters, the so-called space vector modulation [9] will also be considered, together with the need to impose a modulator strategy that can handle the finite switch on/off times of practical converter switches. In this chapter, a set of build and play tutorials are outlined, which will allow the reader to become better acquainted with the subject matter presented in this chapter.
2.2 Single-Phase Half-Bridge Converter

The so-called half-bridge converter configuration as shown in Fig. 2.1 consists of two switches which must be controlled by the modulator. The converter in question is connected to a single-phase symbolic load element $Z$ (see Fig. 2.1).

For drive applications, as considered in this book, the load element is typically a phase of an electrical machine which may be represented by a load impedance in the form of an inductance $L$ and resistance $R$ circuit connected in series, together with a voltage source $e$. The two ideal switches are controlled by two logic signals $Sw_t$, $Sw_b$. Logic 1 corresponds to a closed, i.e., “on”, switch state and logic 0 to an open switch state. There are therefore four possible switch combinations possible as may be observed from Table 2.1. Of the four states shown in Table 2.1, the shoot-through mode must be avoided in voltage source converters, to prevent short-circuiting of the supply. The idle mode is normally used to disable the converter. Observation of Table 2.1 demonstrates that the two active switching states are complementary and can therefore be represented by a single logic switching state $Sw$ with $Sw_t = Sw$ and $Sw_b = \overline{Sw}$.

An example of a typical output voltage waveform, which appears in a half-bridge converter, is given in Fig. 2.2 for the sampling interval $t_{k-1} \ldots t_{k+1}$, where the switching function $Sw$ is assumed to be zero at $t = t_{k-1}$ and changed to its logic state 1 at $t = t_{k-1} + t^r$. Subsequently, $Sw$ is set to zero during the next sample interval at $t = t_k + t^f$, with $t^r$ the instance at which $Sw$ rises and $t^f$ the instance at which $Sw$ falls. This switching sequence is repeated every two samples where $t^r$ and $t^f$ may be varied within the limits of the interval $t_{k-1} \ldots t_k$ and $t_k \ldots t_{k+1}$ respectively. This modulation strategy
Table 2.1  Half-bridge switching states

<table>
<thead>
<tr>
<th>$Sw_a$</th>
<th>$Sw_b$</th>
<th>Voltage $u$</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$-\frac{u_{DC}}{2}$</td>
<td>Idle mode</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>$-\frac{u_{DC}}{2}$</td>
<td>Active mode</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$\frac{u_{DC}}{2}$</td>
<td>Active mode</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$-\frac{u_{DC}}{2}$</td>
<td>Shoot-through mode</td>
</tr>
</tbody>
</table>

is known as double edged PWM, because the rising and falling edge of the load voltage waveform are varied as function of $t^r$ and $t^f$. The latter waveform is also shown in Fig. 2.2 for two samples of operation. They constitute one period $T_{PWM} = 2T_s = 1/f_{PWM}$ of modulator operation.

![Diagram](image)

**Fig. 2.2** Variation of the average voltage per sample, with half-bridge converter

The corresponding average voltage functions $U(t^r)$ and $U(t^f)$ can be found by making use of (2.1), which leads to equation set (2.7)

\[
U(t^r) = \frac{u_{DC}}{2} \left( 1 - \frac{2t^r}{T_s} \right) ; \quad 0 \leq t^r \leq T_s \tag{2.7a}
\]

\[
U(t^f) = \frac{u_{DC}}{2} \left( \frac{2t^f}{T_s} - 1 \right) ; \quad 0 \leq t^f \leq T_s \tag{2.7b}
\]
where $u_{DC}$ represents the DC bus voltage of the converter as shown in Fig. 2.1. Also shown in Fig. 2.2 is a typical load current trajectory in the event that the element $Z$ is represented by an ideal (zero resistance) coil. The gradient of the current waveform is in this case dictated by the ratio $u(t)/L$ while the incremental current change per sample $\Delta i(t_k)$ (which is also shown in Fig. 2.2 for both sample intervals) is determined by the product $U T_s$ (see expression (2.5)).

The average voltage functions according to equation set (2.7) are shown in Fig. 2.3 together with the user defined reference values for both sample intervals. The required switch state $Sw$ may be found by comparing the defined reference average voltage values $U^*(t_{k-1})$, $U^*(t_k)$ (see Fig. 2.3) with the average voltage functions, as defined by equation set (2.7), which leads to the values $t^r$ and $t^f$ needed to meet the condition specified by (2.6). The latter may also be confirmed by observing the green and blue areas shown in the load voltage $u(t)$ waveform which represent the actual voltage–time products $U(t_{k-1}) T_s$ and $U(t_k) T_s$ respectively as generated by the converter. Clearly identifiable in Fig. 2.3 are the switch $Sw$ states over one period of modulator operation, where the red colored interval corresponds to logic level 1.

![Double edged PWM strategy, with half-bridge converter](image)

**Fig. 2.3** Double edged PWM strategy, with half-bridge converter
A generic implementation of a *double edged* PWM strategy, as given in Fig. 2.4, shows two A/D modules which are tied to the reference average voltage value (from the controller) and the measured DC bus voltage $u_{DC}$ value (from the converter module). The sampled DC voltage is multiplied by a gain $1/2$ to provide the maximum sampled average voltage value $u_{DC}/2$. This value is multiplied by a *triangular* function which results in the function $U(t)$ defined by expression equation set (2.7). A summation module compares the two average voltage values $U$ and $U^*$. Its output $\varepsilon$ is used by a so-called comparator module with a transfer function of the form given by equation set (2.8).

$$
\begin{align*}
\text{if } \varepsilon > 0 & \quad \text{comparator output} = 1 \\
\text{if } \varepsilon \leq 0 & \quad \text{comparator output} = 0
\end{align*}
$$

The output of the comparator, known as switching function $S_w$, drives the two converter switches as discussed previously. Note that use of the measured DC bus voltage in the generic structure is beneficial because this provides the modulator with the capability to maintain the average voltage reference value, even when bus voltage variations occur.

![Fig. 2.4 Generic model of double edged PWM based half-bridge modulator](image)

Prior to introducing the full-bridge converter, it is helpful to introduce two modulation parameters which are applicable to sinusoidally varying average voltage reference signals that are commonly used in drive application. The first, known as the *amplitude modulation ratio* $m_A$, is defined as

$$
m_A = \frac{\hat{U}^*}{u_{DC}/2}
$$

where $\hat{U}^*$ represents the peak value of the reference average phase voltage. The second modulation parameter in use is the *frequency modulation ratio* $m_f$ which is defined as
where \( f_{PWM} \) represents the frequency of the triangular waveform shown in Fig. 2.3, which is half the sample frequency \( f_s = 1/T_s \). The frequency of a sinusoidally varying average voltage reference signal is defined as \( f^* \). In Tutorial 2.6.1, located at the end of this chapter, a simulation example is presented to underline the concepts presented in this section.

### 2.3 Single-Phase Full-Bridge Converter

The full-bridge, otherwise known as H-bridge converter, can be constructed by two half-bridge converters as shown in Fig. 2.3. A single-phase load impedance \( Z \) (as defined in the previous section) is again assumed, which in this case is represented by a virtual two-phase equivalent load, with a per phase impedance of \( Z/2 \) and phase currents \( i_1 = i, i_2 = -i \). Use of a virtual two-phase load is particularly instructive for the development of a modulator structure given that this approach can be readily extended to three-phase systems. The virtual two-phase center point voltage with respect to the zero volt node is defined as \( u_0 \).

![H-bridge converter](image)

**Fig. 2.5** H-bridge converter

The key to determining the modulator strategy for this converter centers on the use of (2.1) which, with the aid of Fig. 2.5, may be written as
\[ U(t_k) = \frac{1}{T_s} \int_{kT}^{(k+1)T} u_1(t) \, dt - \frac{1}{T_s} \int_{kT}^{(k+1)T} u_2(t) \, dt. \tag{2.11} \]

In expression (2.11), the terms \( U_1(t_k) \) and \( U_2(t_k) \) are introduced which represent the average (per sample) voltages for both virtual phases. These may in turn be written as

\[ U_1(t_k) = \frac{1}{T_s} \int_{kT}^{(k+1)T} u_a(t) \, dt - \frac{1}{T_s} \int_{kT}^{(k+1)T} u_0(t) \, dt \tag{2.12a} \]
\[ U_2(t_k) = \frac{1}{T_s} \int_{kT}^{(k+1)T} u_b(t) \, dt - \frac{1}{T_s} \int_{kT}^{(k+1)T} u_0(t) \, dt \tag{2.12b} \]

where \( U_a(t_k) \) and \( U_b(t_k) \) represent the half-bridge average voltage values. The required half-bridge average voltage references \( U^*_a(t_k) \), \( U^*_b(t_k) \) can with the aid of equation set (2.12), be written in terms of the user defined average voltage references \( U^*_1(t_k) \), \( U^*_2(t_k) \) as

\[ U^*_a(t_k) = U^*_a(t_k) + U^*_0(t_k) \tag{2.13a} \]
\[ U^*_b(t_k) = U^*_b(t_k) + U^*_0(t_k). \tag{2.13b} \]

In reality, a single-phase load exists, as mentioned above, to which a specified average voltage (per sample) value must be applied and this value is, according to (2.11), given by

\[ U^*(t_k) = U^*_1(t_k) - U^*_2(t_k) \tag{2.14} \]

which, with the aid of equation set (2.13), may also be written as

\[ U^*(t_k) = U^*_a(t_k) - U^*_b(t_k). \tag{2.15} \]

Equation (2.15) shows that the virtual average voltage value \( U^*_0(t_k) \) may be chosen freely (given that it is not present in this equation). This can also be observed from Fig. 2.6(a) where within two consecutive sample intervals the virtual average voltage value \( U^*_0(t_k) \) is arbitrarily selected at values greater and less than zero respectively, for the same average voltage reference value, i.e., \( U^*(t_{k-1}) = U^*(t_k) \). An observation of Fig. 2.6(a) shows that the output pulses correspond to the required average voltage–time reference values \( U^*(t_{k-1})T_s \) and \( U(t_k)T_s \), which in this example were chosen equal. The relative position of the output pulses within the sampling interval is defined by the virtual average voltage values \( U^*_0(t_{k-1}) \) and \( U^*_0(t_k) \). In this example, the values are arbitrarily chosen to be positive and negative respectively. Also
shown in Fig. 2.6 are the half-bridge voltages $u_a$ and $u_b$ which toggle between $\pm \frac{u_{DC}}{2}$.

From a practical perspective, it is prudent to choose the average voltage converter references $U^*_a(t_k)$ and $U^*_b(t_k)$, during each sample interval in such a manner that they are symmetrically oriented with respect to the horizontal time axis. If this condition is maintained, the largest possible value of
$U^* = u_{DC}$ may be realized by the modulator/converter. Symmetrical orientation of the references $U^*_a(t_k)$ and $U^*_b(t_k)$ can be achieved by imposing the condition

$$\max \{U^*_a(t_k), U^*_b(t_k)\} + \min \{U^*_a(t_k), U^*_b(t_k)\} = 0. \quad (2.16)$$

With the aid of (2.13), this expression may also be written as

$$\max \{U^*_1(t_k), U^*_2(t_k)\} + \min \{U^*_1(t_k), U^*_2(t_k)\} + 2U^*_0(t_k) = 0 \quad (2.17)$$

which fully defines the required virtual average voltage reference level $U^*_0(t_k)$ needed to satisfy (2.16). The control structure, which is referred to as a pulse centering unit and corresponds to (2.13) and (2.17), is given in Fig. 2.7.

![Fig. 2.7 Pulse centering module](image)

Note that for the full-bridge modulator considered here, expression (2.16) may be written as

$$U^*_a(t_k) + U^*_b(t_k) = 0 \quad (2.18)$$

which symmetrizes the references with respect to the time axis. Input to the pulse centering reference value are the variables $U^*_1$ and $U^*_2$ while the input to the modulator is equal to $U^*$ which, according to (2.14), is equal to the difference of said variables. Correspondingly, one of the two reference values can be chosen arbitrarily and a convenient choice is as follows

$$U^*_1(t_k) = U^*(t_k) \quad (2.19a)$$
$$U^*_2(t_k) = 0. \quad (2.19b)$$

The outputs from the pulse centering module are therefore of the form
\[ U^*_a(t_k) = \frac{1}{2} U^*(t_k) \quad (2.20a) \]

\[ U^*_b(t_k) = -\frac{1}{2} U^*(t_k). \quad (2.20b) \]

Figure 2.6(b) shows the impact of choosing the average voltage value \( U_0 \) according to (2.17). Observation of the load voltage waveform demonstrates that it has now been centered with respect to the middle of the sample interval. Consequently, increasing the value of the reference average voltage value \( U^* \) will increase the area underneath the voltage pulse, but its position relative to the sampling interval remains unchanged. Without the use of this pulse centering unit an increase in the reference \( U^* \) will lead to a situation where one of the half-bridge references will exceed the maximum value. For example, reference \( U^*_a \) in Fig. 2.6(a) will exceed the absolute maximum value before reference \( U^*_b \). With pulse centering, both half-bridge average voltage reference values will remain centered. Hence, they will reach their maximum value simultaneously.

A generic representation of the modulator for the H-bridge converter topology, is given in Fig. 2.8 and contains two comparators which provide the logic signals \( S w^a \) and \( S w^b \) that are in turn used to control the switches as discussed in the previous section. The tutorial given in Sect. 2.6.3 shows the use of the generic H-bridge modulator with a full-bridge converter connected to an inductive load.

**Fig. 2.8** Generic model of double edged PWM based modulator for full-bridge converter
2.4 Three-Phase Converter

The three-phase converter topology, as shown in Fig. 2.9, consists of a symmetric balanced star connected load which is connected to three half-bridge converters as discussed in Sect. 2.2. The converter structure is similar to the virtual two-phase structure introduced in the previous section. Accordingly, the mathematical handling required to obtain the average voltage references for the three half-bridges is very similar as will become apparent shortly. The aim is to determine (for a given sampling interval) a switching strategy for the six switches of the converter, which ensures that the average load phase voltage values \( U_1(t_k), U_2(t_k), U_3(t_k) \) correspond with the three reference values \( U_1^*(t_k), U_2^*(t_k) \) and \( U_3^*(t_k) \). The latter are in turn linked to the (power invariant) space vector average voltage reference value \( \vec{U}^* \) as given in (2.21), in its sampled form

\[
\vec{U}^*(t_k) = \sqrt{\frac{2}{3}} (U_1^*(t_k) + U_2^*(t_k) e^{j\gamma} + U_3^*(t_k) e^{2j\gamma})
\]  

(2.21)

where \( \gamma = \frac{2\pi}{3} \). Furthermore, a modulator generic structure is to be developed to produce the required switching signals for the converter on the basis of the user defined average voltage reference vector \( \vec{U}^* \).

![Fig. 2.9 Three phase converter](image)

The average voltage (per sample) values for the three-phase load can, with the aid of (2.1) and Fig. 2.9, be written as...


\[ U_1^* (t_k) = \frac{1}{T_s} \int_{t_k}^{t_k+T_s} u_a (t) \, dt - \frac{1}{T_s} \int_{t_k}^{t_k+T_s} u_o (t) \, dt \] (2.22a)

\[ U_2^* (t_k) = \frac{1}{T_s} \int_{t_k}^{t_k+T_s} u_b (t) \, dt - \frac{1}{T_s} \int_{t_k}^{t_k+T_s} u_o (t) \, dt \] (2.22b)

\[ U_3^* (t_k) = \frac{1}{T_s} \int_{t_k}^{t_k+T_s} u_c (t) \, dt - \frac{1}{T_s} \int_{t_k}^{t_k+T_s} u_o (t) \, dt \] (2.22c)

where \( U_a(t_k), U_b(t_k) \) and \( U_c(t_k) \) represent the three half-bridge average voltages values. The required half-bridge average voltage references \( U_a^* (t_k), U_b^* (t_k) \) and \( U_c^* (t_k) \) can, with the aid of equation set (2.22), be written in terms of the user defined average voltage references \( U_1^* (t_k), U_2^* (t_k) \) and \( U_3^* (t_k) \) as

\[ U_a^* (t_k) = U_1^* (t_k) + U_o^* (t_k) \] (2.23a)

\[ U_b^* (t_k) = U_2^* (t_k) + U_o^* (t_k) \] (2.23b)

\[ U_c^* (t_k) = U_3^* (t_k) + U_o^* (t_k) \] (2.23c)

which contains a zero sequence average voltage (per sample) value \( U_o^* (t_k) \) that can be defined in terms of the user defined average voltage values according to the approach set out in the previous section. In practice, it is helpful to rewrite equation set (2.23) in a space vector format. Using equation set (2.23) and (2.21) gives

\[ \bar{U}^* (t_k) = \sqrt{\frac{2}{3}} \left( U_a^* (t_k) + U_b^* (t_k) e^{j\gamma} + U_c^* (t_k) e^{2j\gamma} \right) - \sqrt{\frac{2}{3}} U_o (t_k) \left( 1 + e^{j\gamma} + e^{2j\gamma} \right) \] (2.24)

The second term of expression (2.24) contains a vector sum of value zero, together with the zero sequence average voltage value \( U_o^* (t_k) \), which implies that the latter can be chosen freely. It is noted that the approach discussed here is almost identical to that used in the previous section. The choice of the zero sequence average voltage value is therefore of no concern with respect to the choice of the average voltage half-bridge references. However, it is prudent to choose the value of \( U_o (t_k) \) in such a manner that the maximum and minimum value of the half-bridge reference values are symmetrical with respect to the time axis. The reader is reminded of the fact that this same approach was purposefully introduced for the full-bridge modulator, which led to condition 2.16. This condition can simply be adapted to accommodate three instead of two variables allowing this expression to be written as
\[
\max \{ U_a^* (t_k), U_b^* (t_k), U_c^* (t_k) \} \\
+ \min \{ U_a^* (t_k), U_b^* (t_k), U_c^* (t_k) \} = 0. 
\]

(2.25)

With the aid of equation set (2.23), this expression may also be written as
\[
\max \{ U_1^* (t_k), U_2^* (t_k), U_3^* (t_k) \} \\
+ \min \{ U_1^* (t_k), U_2^* (t_k), U_3^* (t_k) \} + 2U_o^* (t_k) = 0. 
\]

(2.26)

Further development of (2.26) gives
\[
U_o^* (t_k) = -\frac{1}{2} [\max \{ U_1^* (t_k), U_2^* (t_k), U_3^* (t_k) \} \\
+ \min \{ U_1^* (t_k), U_2^* (t_k), U_3^* (t_k) \}] 
\]

(2.27)

which fully defines the zero sequence average voltage value \( U_o^* (t_k) \) for each sampling interval. The pulse centering unit according to Fig. 2.7 is readily modified to a three output/three input structure, as given in Fig. 2.10 that complies with (2.27).

![Fig. 2.10 Three-phase pulse centering module](image)

An example which demonstrates the omission and use of the pulse centering unit is given in Fig. 2.11 for the case where a reference vector \( \vec{U}^* (t_i) \) of constant amplitude \( \sqrt{3/8} u_{DC} \) is rotated by \( \pi/6 \) rad during a time interval \( T_s \). The angle \( \rho^* (t_i) \) between the reference vector and the real axis of a stationary complex plane is chosen to be zero at time \( t_{k-1} \), i.e., \( \rho^* (t_{k-1}) = 0 \). The corresponding average load voltage reference values \( U_{1,2,3}^* \) for each sampling
interval may be found via a standard power invariant vector to three-phase conversion, which gives

\[ U_1^* (t_i) = \sqrt{\frac{2}{3}} \Re \{ \vec{U}^* (t_i) \} \]  

\[ U_2^* (t_i) = \sqrt{\frac{2}{3}} \Re \{ \vec{U}^* (t_i) e^{-j\gamma} \} \]  

\[ U_3^* (t_i) = \sqrt{\frac{2}{3}} \Re \{ \vec{U}^* (t_i) e^{-j2\gamma} \} . \]  

Application of equation set (2.28) to the chosen reference vector for the two samples leads to the reference phase values given in Table 2.2, which also gives the value of \( U_0^* \) as calculated using (2.27). Note from Table 2.2 that the choice of reference space vector amplitude \( |\vec{U}^*| = \sqrt{3/8} u_{DC} \) is such that the phase variable \( U_1^* (t_k) \) is at the highest possible value of \( 1/2 u_{DC} \). This implies that the largest orbit of the reference vector that can occur \textit{without} pulse centering may be represented by a circle with radius \( \sqrt{3/8} u_{DC} \). The required half-bridge average voltage values \( U_{a,b,c}^* \) may be found with the aid of the pulse centering module given in Fig. 2.10 in which case the zero sequence average voltage reference value \( U_0^* \) is calculated using (2.27).

<table>
<thead>
<tr>
<th>Phase reference</th>
<th>Time ( t_{k-1} )</th>
<th>Time ( t_{k1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( U_1^* )</td>
<td>( 1/2 u_{DC} )</td>
<td>( \sqrt{3/2} u_{DC} )</td>
</tr>
<tr>
<td>( U_2^* )</td>
<td>( -1/4 u_{DC} )</td>
<td>0</td>
</tr>
<tr>
<td>( U_3^* )</td>
<td>( -1/4 u_{DC} )</td>
<td>( -\sqrt{3/2} u_{DC} )</td>
</tr>
<tr>
<td>( U_0^* )</td>
<td>( -1/8 u_{DC} )</td>
<td>0</td>
</tr>
</tbody>
</table>

In the first diagram, Fig. 2.11(a), no pulse centering is used, i.e., \( U_0^* \) has been set to zero. An observation of the example given in Fig. 2.11(b) shows that the pulse centering unit symmetrizes the maximum and minimum average voltage references \( U_{a,b,c}^* \) with respect to the time axis. The use of the pulse centering unit has, as may be observed from Fig. 2.11(b), lowered the \( U_1^* (t_k) \) value to \( 3/8 u_{DC} \) which implies that the average voltage reference vector amplitude may be further increased before reaching the supply voltage limits \( \pm u_{DC}/2 \) of the converter. It will be shown in the next subsection that the introduction of pulse centering allows the user to increase the reference space vector amplitude from \( |\vec{U}^*| = \sqrt{3/8} u_{DC} \) to \( |\vec{U}^*| = \sqrt{1/2} u_{DC} \), which is an increase of approximately 15%. For the second sample \( t_k \ldots t_{k+1} \), the half-bridge average voltage reference values were already balanced with respect to the time axis, which implies that the waveforms for this sample are identical to those shown in Fig. 2.11(a) for interval \( t_k \ldots t_{k+1} \). Also shown in Fig. 2.11 are the half-bridge voltages \( u_a, u_b, u_c \) which toggle between \( \pm u_{DC}/2, \)
with respect to the zero bus voltage node. In addition, the three comparator output switch states $Sw^a$, $Sw^b$, $Sw^c$ are shown in Fig. 2.11.

![Asymmetrically sampled PWM, three-phase converter, use of pulse centering unit](image)

**Fig. 2.11** Asymmetrically sampled PWM, three-phase converter, use of pulse centering unit

The generic diagram for the three-phase converter as given in Fig. 2.12 is similar to the modulator concept described for the single-phase full-bridge converter. However, in this case the pulse centering module is used to generate
the average voltage reference value for the three half-bridges on the basis of the user defined space vector average voltage reference.

![Generic model of double edged PWM based modulator for three-phase converter](image)

**Fig. 2.12** Generic model of double edged PWM based modulator for three-phase converter

### 2.4.1 Space Vector Modulation

It is also helpful to consider the above modulator scheme from a space vector perspective. The so-called *space vector modulation*, introduced by van der Broeck et al. [9], is directly based on the use of (2.21). Using a pulse centering unit is important to maximize the linear operating region of the converter. Hence, further discussion will focus on Fig. 2.11, which also shows the switch states that correspond with this example. These switch states and corresponding half-bridge converter outputs can, with the aid of (2.21), be interpreted as a set of voltage space vectors. The switch states shown in Fig. 2.11 represent a subset of the eight possible converter switching combinations \( \{ S_{w^a}, S_{w^b}, S_{w^c} \} \) which gives

\[
\bar{u}_{\{ S_{w^a}, S_{w^b}, S_{w^c} \}} = \sqrt{\frac{2}{3}} u_{DC} \left\{ S_{w^a} + S_{w^b} e^{j\gamma} + S_{w^c} e^{j2\gamma} \right\}. \tag{2.29}
\]

Evaluation of (2.29) shows that there are six active voltage vectors of magnitude \( \sqrt{2/3} u_{DC} \) that are displaced by \( \pi/3 \) rad as indicated in Fig. 2.13. In addition, two zero vectors are present in this figure corresponding to converter
switch combinations \{000\} and \{111\}. The process by which the converter meets the condition specified by (2.30) may therefore be interpreted in terms of determining the two active voltage vectors adjacent to the reference average voltage vector \(\vec{U}^*\) and determining the time interval for which they must be active during the sampling time \(T_s\). In addition, the duration of the zero vectors must be determined for each sampling interval.

\[
\vec{U}(t_i) = \vec{U}^*(t_i) \tag{2.30}
\]

A mathematical formulation of this strategy is of the form

\[
\vec{U}^*(t_i) = \left(\frac{T_{a1}(t_i)}{T_s}\right) \vec{u}_\pi + \left(\frac{T_{a2}(t_i)}{T_s}\right) \vec{u}_e e^{j\frac{\pi}{3}} \tag{2.31}
\]

where \(\vec{u}_\pi\) is, according to (2.29), the active voltage vector which falls within the angle interval \(\rho^*(t_i)\). In addition, the total duration of the time during which the active vectors can be deployed must satisfy the condition given in (2.32).

\[
\frac{T_{a1}(t_i)}{T_s} + \frac{T_{a2}(t_i)}{T_s} \leq 1 \tag{2.32}
\]

The equivalent space vector representation for the example discussed in the previous section with the aid of Fig. 2.11 is shown in Fig. 2.13. Included in both sub-figures are the eight possible converter voltage space vectors, together with the average voltage reference vectors for both samples \(t_{k-1}\) and \(t_k\). The active voltage converter vector \(\vec{u}_\pi\), which must be used with (2.31), is in this case \(\vec{u}_{\{100\}}\). Figure 2.13 shows that the PWM approach outlined earlier in this section determines the appropriate duration times for the active vectors as to satisfy equation set (2.31) and (2.32). Furthermore, the presence of the pulse centering unit ensures that the combined time interval in which active vectors are used is centered with respect to the center of the sampling interval. For the first sample \(t_{k-1} \ldots t_k\), the average voltage reference vector coincides with the active average voltage converter vector \(\vec{U}_{\{100\}}\). In this case, the modulation strategy determines the required time needed to activate said vector during the sample interval. For the second sample interval, two active vectors adjacent to the average voltage reference vector are activated for a time interval sufficient to ensure that the condition given by (2.30) is met.

It is emphasized that the modulation technique discussed above determines, on the basis of the reference voltage, the duration of the active vectors used within each sample. Furthermore, the pulse centering unit is responsible for centering the combined active vector time interval within the sample. An often quoted alternative to the strategy discussed above, is the so-called space vector modulation [9] which is particularly suited to digital implementation as this approach calculates directly for a given sample interval \(t_i\) the duration of the active vectors adjacent to the specified average voltage reference vector \(\vec{U}^*(t_i)\) with the aid of equation set (2.33), namely
These expressions can be found using (2.31) and (2.32) and gives the user access to the required duration time of the active vectors, without having to implement a generic modular structure as given by, for example, Fig. 2.12.

The centering of the combined active time interval must however be carried out ensuring that a zero vector (if needed) is activated for the same time interval at the beginning and end of each sample interval. The choice of zero vectors used at any particular instance is decided on the basis of a minimum number of switch actions needed to reach the nearest zero vector from the last active vector in use. In terms of modulation, the overall result achieved with space vector modulation is identical in its execution to the pulse width modulation strategy as undertaken with the aid of the generic modulator structure given by Fig. 2.12.

Finally, it is considered important to determine the maximum reference average voltage amplitude \( \{ U^* (t_i) \}^{\text{max}} \) which may be used without imposing any constrains on the corresponding phase angle \( \rho^* (t_i) \). Substitution of the active vector \( \bar{u}_\pi \) (see (2.29)) into equation set (2.33) leads, after some mathematical manipulation, to

\[
\left( \frac{T_{a1} (t_i)}{T_s} \right)^2 + \frac{T_{a2} (t_i)}{T_s} + \left( \frac{T_{a2} (t_i)}{T_s} \right)^2 = \left( \frac{2 U^* (t_i)}{\sqrt{3} u_{\text{DC}}} \right)^2 \quad (2.34)
\]
in which the active vector \( \vec{u}_s \) is arbitrarily chosen as \( \vec{U}_{(100)} \). Equation (2.34) represents an ellipse in the \( T_{a1}/T_s, T_{a2}/T_s \) plane and its size is determined by the variable \( \nu = U^*(t_i)/\sqrt{\frac{3}{2}}u_{DC} \) as may be observed from Fig. 2.14.

\[
\frac{T_{a1}(t_i)}{T_s} + \frac{T_{a2}(t_i)}{T_s} = 1
\]

\[
\frac{U^*(t_i)}{\sqrt{\frac{3}{2}}u_{DC}} = \sqrt{\frac{3}{4}}
\]

\[
\frac{U^*(t_i)}{\sqrt{\frac{3}{2}}u_{DC}} = \frac{3}{4}
\]

**Fig. 2.14** Active vector duty cycles for \( \nu = \frac{3}{4} \) and \( \nu = \sqrt{\frac{3}{4}} \)

Figure 2.14 shows how the duty cycle of two adjacent active vectors can be selected to achieve a given voltage reference value \( U^* \) (amplitude only) as expressed by the variable \( \nu \). Also shown in this diagram is a straight line which represents the sum of the two duty cycles which must be equal to one. Indeed, the time over which both vectors are activated cannot exceed the sample interval \( T_s \). Observation of Fig. 2.14 shows two curves with values of \( \nu = \frac{3}{4} \) and \( \nu = \sqrt{\frac{3}{4}} \) corresponding to a voltage reference amplitude of \( U^* = \sqrt{\frac{3}{8}} u_{DC} \) and \( U^* = \sqrt{\frac{1}{2}} u_{DC} \) respectively. The latter value is the largest reference value which can be produced given that it corresponds with the largest ellipse (shown partly in the first quadrant) that can be used, given the constraints imposed by the linear function and two axes shown in Fig. 2.14. For comparison purposes part of a second ellipse (dotted curve) has also been drawn in Fig. 2.14. This ellipse corresponds to the largest ellipse with reference voltage \( \sqrt{\frac{3}{8}} u_{DC} \) that can be used without the presence of a pulse centering module whilst maintaining the phase references within the supply limits \( \pm u_{DC}/2 \). This leads to an important observation, namely that centering the active vectors within a sample either by use of a pulse centering PWM unit or by calculation using the space vector modulation approach allows the user to extend the linear operating range by a factor of \( \frac{2}{\sqrt{3}} \simeq 15\% \), without encountering the supply level limits of the converter. Note that the ability to extend the linear operation of the modulator/converter by approximately 15% is particular advantageous as it allows the converter to be operated with higher voltages and consequently lower currents. The latter implies that the kVA-rating of the converter can be increased by approximately 15% as a result of using pulse centering.
It is instructive to consider the circuit orbit which coincides with the highest allowable reference value, as discussed above, in a diagram together with the converter active and zero vectors. Such a diagram is given in Fig. 2.15 and shows that the circular orbit is the largest which can be located within a hexagon that is constructed from the six active vectors with length $\sqrt{2/3} \, u_{\text{DC}}$. Observation of Fig. 2.15 shows the presence of a right-angled triangle of which the hypotenuse is represented by the active vector $\vec{u}_{\{100\}}$ and one of the legs which represents the radius $u_{\text{DC}}/\sqrt{2}$ of the circle. The triangle in question is a $30^\circ$–$60^\circ$–$90^\circ$ acute triangle, of which the sides are in the ratio $1 : \sqrt{3} : 2$. This also shows that the largest circle which can be placed inside the hexagon must have a radius that is $\sqrt{3}/2$ smaller than the active vector amplitude.

Prior to considering the effect of dead time on the converter, it is instructive to examine a scenario where the reference voltage vector amplitude is increased beyond the maximum value of $u_{\text{DC}}/\sqrt{2}$. Under such conditions, the half-bridge reference values will exceed the DC supply limits during part of the circular orbit undertaken by the reference vector. This implies that the converter output voltage(s) may be held to the supply value for a period of time which is in excess of the sampling time. Consequently, the converter switching frequency will no longer be equal to half the sampling frequency. This mode of operation is referred to as over-modulation and will ultimately
lead (with increasing $U^*$) to a situation where the converter waveforms are rectangular. In vector terms, this operation is characterized by switching from one active vector to the next, i.e., along the hexagon boundary shown in Fig. 2.15. This mode of operation is known as six-step operation and can be readily observed by increasing the reference voltage amplitude beyond the value $u_{dc}/\sqrt{3}$ in the tutorial given in Sect. 2.6.5.

2.5 Dead-Time Effects

In the converter configuration shown in this chapter ideal switches were used, which implies that they may be turned on or off instantaneously. Consequently, the on and off switch signals were chosen complimentary (one signal set to logical 1, the other to logical 0), as shown in Fig. 2.3. In reality, semiconductor based switches and diodes are used which require a finite turn-on and turn-off time. This implies that a so-called dead time $\Delta t_D$ must be imposed, which is the time when both switch signals are set to zero, to allow the switch turn-on/-off process to be completed. Failure to adhere to this policy can invoke the shoot-through mode as identified in Table 2.1 with usually disastrous consequences for the devices in question. The half-bridge configuration shown in Fig. 2.16 is representative of the converter topologies discussed in this section. Shown in Fig. 2.16 are two IGBT switches with corresponding diodes which are taken to be non-ideal, i.e., these require a finite turn-on/off time taken to be equal to $\Delta t_D$.

![Fig. 2.16 IGBT based half-bridge converter with power source and modulator](image-url)
Consequently, the question arises how for example the generic modulator structure according the Fig. 2.4 may be modified to accommodate a dead time equal to at least $\Delta t_D$. This technique can subsequently be equally applied to the full-bridge and three-phase converter. The envisaged approach is to introduce two comparators (to control the switches individually) and adding an average voltage offset $\pm U_D/2$ to the reference voltage value $U^*$ as shown in Fig. 2.17. The value of $U_D$ is defined as

$$U_D = u_{DC} \frac{\Delta t_D}{T_s}$$

(2.35)

which may be found by considering the absolute gradient of the function $U(t)$ which is equal to $u_{DC}/T_s$. The value of $\pm U_D/2$ and corresponding dead-time value shown in Fig. 2.17 is purposely chosen large, in comparison to the sample time $T_s$ for didactic reasons.

The consequence of introducing converter dead time is that the modulator will not be able to set the control signals in such a manner that the delivered
average voltage–time area to the load (per sample interval) is exactly equal
to the reference average voltage–time area (see (2.6)). The reason for this
effect may be illustrated with the aid of Fig. 2.17, which shows two examples
where the reference average voltage level is purposely kept constant. In the
first example given in Fig. 2.17(a), the load current is assumed to be negative
and the load will be connected to the negative DC rail voltage as long as the
bottom switch is closed. However, when the switch signal for this device is
set to zero the turn-off process will start and the current will be commutated
immediately to the top diode. This implies that the load is connected to the
top supply rail during the dead-time period. After this dead-time interval
the top switch is activated which means that the load remains connected
to the top rail either by virtue of negative current through the top diode or
positive current through the (conducting) top switch. In this case, the average
voltage (per sample) across the load is larger than the required reference
average voltage level as shown by (2.36a). In the second example, shown in
Fig. 2.17(b), a positive load current is assumed and events as described for the
previous interval also occur with the difference that the bottom diode will
remain conducting during the dead-time interval when the bottom switch
turns off. Likewise, the bottom diode will also conduct during the dead-time
interval as soon as the top switch turns off. Figure 2.17(b) demonstrates that
the average voltage across the load will be less than the required reference
average voltage value. The impact of the dead-time effect on the average load
voltage may be observed with the aid of (2.36).

\[
U = U^* + \frac{U_D}{2} \quad (i < 0) \tag{2.36a}
\]

\[
U = U^* - \frac{U_D}{2} \quad (i > 0) \tag{2.36b}
\]

Observation of equation set (2.36) and (2.35) shows that the error in the
average load voltage with respect to the reference average load voltage de-
dpends on the polarity of the load current as well as the ratio between dead
time and sample time. The dead time is a semiconductor device dependent
variable (typically set to a constant, safe value), whereas the sample time
may be chosen by the user. If the sample frequency \( f_s = 1/T_s \) is increased,
the ratio \( \Delta t_D/T_s \) increases and consequently a larger average voltage er-
ror \( U_D/2 \) is introduced. In the tutorial section at the end of this chapter
a simulation is shown (see Sect. 2.6.2) which demonstrates the issues set
out in this subsection. Dead-time effects are not, for didactic reasons, in-
cluded in the modulation strategies to be discussed in the remaining part of
this book. However, dead-time effects must be accommodated in a practical
power electronic converter using, for example, the techniques outlined in this
section.
2.6 Tutorials

2.6.1 Tutorial 1: Half-Bridge Converter with Pulse Width Modulation

This tutorial is concerned with the implementation of a half-bridge converter structure as given in Fig. 2.1. The ideal switches are to be replaced by a combination of ideal semiconductors and diodes as shown in Fig. 2.16. A supply voltage \( u_{DC} = 300 \text{ V} \) is assumed together with an impedance \( Z \) which in this case is reduced to an ideal inductance of 100 mH. A modulator structure as shown in Fig. 2.4 is to be implemented with a sample interval setting of \( T_s = 1 \text{ ms} \). Furthermore, a sinusoidal 50 Hz reference average voltage waveform \( U^* \) with an amplitude of 100 V is to be used. The aim is to implement a simulation model and examine the sampled reference average voltage, voltage/current waveforms linked to the load, as well as the logic switch signals for this model. A 20 ms simulation time interval is to be used.

Fig. 2.18 Simulation of half-bridge converter with PWM

An example of a simulation model which satisfies the needs for this tutorial is given in Fig. 2.18. Readily identifiable in this figure is the converter topology which consists of two ideal IGBT’s and ideal diodes. The modulator structure is consistent with the generic structure shown in Fig. 2.4. An \textit{enable} module is used together with a logic interface unit to activate the converter from time mark \( t = 1 \text{ ms} \) onwards. Such a logic interface is usually implemented to ensure that the modulator circuit is enabled prior to the converter, to reduce the risk of accidental activation of both switches simultaneously during the power-up phase of operation.

The scope 5 waveforms in Fig. 2.19 represent the voltage across the load inductance and corresponding load current (depicted with a different amplitude scale). Observation of the load current waveform shows the presence of a series of incremental current steps. Two incremental current steps are made during each sample interval. The algebraic sum of each two steps is
defined by the load average voltage–time product \( U(t_k) T_s \) (for a given load inductance value \( L \)) as shown earlier in Fig. 2.2. If the modulator operates correctly, the load average voltage \( U_{\text{conv}}(t_k) \) must be equal to the sampled reference average voltage \( U^*(t_k) \). Both signals are shown in scope module 2. For this purpose, a module \( \bar{x} \) is introduced in the simulation which calculates the average voltage per sample time on the basis of the instantaneous input value, which is in this case the voltage across the load. Note that the output voltage of the \( \bar{x} \) module corresponds to the calculated average voltage value of the previous sample. The two complimentary switch signals given in scope modules 3 and 4 are directly tied to the comparator signal \( Sw \). The ideal switches which are controlled by the signals \( Sw_1, Sw_2 \) (logic one corresponds to a switch on-state) connect the converter center node to the appropriate supply rail as shown in scope 5. The modular switch signal \( Sw \) is in turn determined by the average voltage function \( U(t) \) and the sampled reference average voltage \( U^*(t_k) \) shown in scope module 1.
2.6.2 Tutorial 2: Half-Bridge Converter with PWM and Dead-Time Effects

This tutorial considers the effects of dead time as discussed in Sect. 2.5. For this purpose the tutorial exercise as discussed above should be modified to accommodate an unrealistically high dead time of $\Delta t_D = 100\,\mu s$, which, according to (2.35), corresponds to a band value $U_D$ of 30 V, given the supply voltage and sample time value introduced in the previous section. Note that the dead-time value has been purposely chosen high to better illustrate the effect of including this phenomenon in the simulation. A CASPOC based implementation example which satisfies this tutorial is given in Fig. 2.20 and is unchanged with respect the previous tutorial in terms of average voltage reference, assumed load and DC supply value. A full-bridge logic interface module is used to provide the appropriate switching signals for the two switches. The error input to two comparators is an error signal which is formed by the PWM signal $U(t)$ and the sampled average voltage reference value. The latter is offset by a value of $\pm 15\,V$ in order to realize the required dead-time average voltage band value of $U_D = 30\,V$. Again, a $\bar{x}$ module has been added to this simulation which calculates the actual converter average voltage per sample value.

![Diagram](image-url)

**Fig. 2.20** Simulation of half-bridge converter with PWM and dead-time effects

The waveforms generated by the simulation are again shown in Fig. 2.21. The waveforms given in scope 3 show that the switching signals for the converter are no longer complimentary. Instead a dead-time interval $\Delta t_D = 100\,\mu s$ is present between the two signals in question in order to facilitate the turn-on and turn-off sequence of the devices. The effects of including this dead time on, for example, the load voltage while changing polarity of the
Fig. 2.21 Simulation results for half-bridge converter with PWM

Load current may be observed in scope 2, by comparing the average voltage value (calculated by the \( \bar{x} \) module) with the sampled reference voltage value.
2.6 Tutorials

2.6.3 Tutorial 3: Full-Bridge Converter with Pulse Width Modulation

This tutorial is concerned with a full-bridge converter concept as discussed in Sect. 2.3. For this purpose, the half-bridge based tutorial as discussed in Sect. 2.6.1 is to be modified to accommodate the new converter topology and the generic modulator structure shown in Fig. 2.8. The average voltage reference, load and supply variables remain unchanged with respect to those discussed in tutorial 1. However, to better understand the role of pulse centering, the voltage references $U_1^*$, $U_2^*$, shown in Fig. 2.8, are to be provided by a two-phase pulse centering module as shown in Fig. 2.7. Inputs to this module are the voltage references $U_1^*$, $U_2^*$. The voltage reference $U_2^*$ is arbitrarily set to zero. Furthermore, a sinusoidal, 50 Hz reference average voltage waveform $U^*$ with an amplitude of 100 V is to be used as introduced in tutorial 1, which will be used to represent $U_1^*$. An on/off switch is introduced to enable or disable the pulse centering unit. Disabling said unit will set the reference voltage $u^*_o$ to zero, otherwise this value is calculated using expression (2.17). The introduction of the switch will enable the user to examine the role of the pulse centering, which is the main goal of this tutorial. The CASPOC based simulation model is given in Fig. 2.22 and clearly shows the use of two half-bridges with the ideal IGBT semiconductors and ideal diodes. A differential voltage probe measures the voltage across the inductive load. Furthermore, an average voltage module is used to calculate the actual average voltage per sample $U_{\text{conv}}$ generated by the converter, so that this value can be compared with the required value during each sample of the simulation. A full-bridge logic interface module has been introduced which houses the logic components as required to generate the semiconductor gate signals from the comparator modules and step module which generates the drive enable signal, as discussed in Tutorial 2.6.2 for a single half-bridge. The pulse centering module used in this simulation model represents the generic structure according to Fig. 2.7, with the minor change that an analog switch has been introduced in the corresponding simulation module to set the output $U_o^*$ to zero when the control input is set to logical zero by way of the on/off toggle switch. Outputs of the pulse centering unit are the two half-bridge reference variables and the variable $U_o^*$, which is particularly instructive, as they show the user how the pulse centering unit calculates this value based on the two reference input values. The remaining part of the modulator circuit is in accordance with the modulator generic diagram given in Fig. 2.8. As with the previous tutorials, a sampling time of $T_s = 1$ ms is assumed.

The waveforms generated by the simulation are shown Fig. 2.23. The load voltage in scope 5 toggles between ±300 V, which is double the value that is achievable with the half-bridge converter. This also means that the maximum average voltage level $U_{\text{max}}$ is doubled when compared to the half-bridge converter topology. Furthermore, it is of interest to run the simulation with and
Fig. 2.22 Simulation of full-bridge converter with PWM

Fig. 2.23 Simulation results for full-bridge converter with PWM
without activation of the pulse centering unit to examine the orientation of the load voltage pulses (see scope 1 voltage waveform) relative to the center of each sampling interval. Observation of the results with the pulse centering unit active shows that the load voltage pulses are indeed centered with respect to the middle of the sample interval, in accordance with the waveforms given in Fig. 2.6(b). Furthermore, it may be verified that the largest reference voltage that can be used in this tutorial (without $U_{\text{a}}^*$, $U_{\text{b}}^*$ exceeding the supply voltage limits of the converter) with and without pulse centering is equal to 150 V and 300 V respectively.

2.6.4 Tutorial 4: Three-Phase Pulse Width Modulator with Pulse Centering

The operation of the pulse centering technique for three-phase pulse width modulators, as discussed in Sect. 2.4 is to be considered in this tutorial. Of interest is to develop a simulation model of the generic structure shown in Fig. 2.12 that is able to generate the switching signals $S_{\text{wa}}$, $S_{\text{wb}}$, $S_{\text{wc}}$ on the basis of a rotating average voltage reference vector $\bar{U}^*(t)$. Furthermore, the required simulation should be able to display the converter voltage space vectors (as given in Fig. 2.15), which are used during each sample time step $T_s$ for the duration of the chosen simulation time, which spans four periods. For this example, the average voltage reference vector at the start of the simulation is set to $\bar{U}^*(t = 0) = \sqrt{3/8} \, u_{\text{DC}}$, with $u_{\text{DC}} = 300$ V, corresponding to the values chosen for the example given in Fig. 2.11 and Fig. 2.13(a). A sample time of $T_s = 1$ ms is assumed together with a fixed amplitude rotating (average) voltage reference vector, with an angular frequency of $\pi/6 \, T_s \, \text{rad/s}$. The latter has been purposely chosen to realize a $30^\circ$ rotation of the vector over each sample interval, which is precisely in accordance with the example used to generate Fig. 2.11 and Fig. 2.13(b). This implies that the tutorial provides an opportunity for the reader to quantitatively verify the example discussed in Sect. 2.4, with and without the use of the pulse centering technique. Note that the selected angular frequency is relatively high in comparison with those used in drive applications. The reason for this is that this tutorial is aimed at showing the user how the converter vectors are generated to deliver the required average voltage vector during each sample interval, with and without the use of pulse centering, as was mentioned above.

The CASPOC based simulation model as given in Fig. 2.24 shows the three-phase modulator with an input in the form of a rotating average voltage vector. The latter is sampled and used with a two- to three-phase (power invariant) conversion module to obtain the three-phase load average voltage reference values $U_1^*$, $U_2^*$, $U_3^*$. The converter reference average voltage variables $U_{\text{a}}^*$, $U_{\text{b}}^*$, $U_{\text{c}}^*$ used during each interval are generated with the submodule Pulse Center Module, the combination of which satisfies equation set (2.23).
The Pulse Center Module, as given in Fig. 2.12 calculates the required zero-sequence reference average voltage value $U_o^*$ which is output variable of this module. A toggle switch is also shown in Fig. 2.24 which allows the user to enable/disable the pulse centering function. Setting the output value of the toggle switch to logic one enables the pulse centering module. With the value set to zero, the pulse centering module sets the zero-sequence reference average voltage to zero, in which case the output are equal to the input variables of the module.

The waveforms generated by the simulation are shown in Fig. 2.25. Observation of the scope 3 vector diagram confirms that the sampled average voltage reference vector rotates from zero to 30° during the first two sample intervals 0 → 2$T_s$ of the simulation. Also shown in this vector diagram
are the converter space vectors used to generate the required average voltage reference vector. In this context, note that converter zero vectors are shown as small circles at the origin. These change to arrow points when a converter active vector is selected during the simulation.

The corresponding switch states $Sw^a, Sw^b, Sw^c$, shown by scope module 2, are in accordance with those shown in Fig. 2.11(a) in case pulse-centering is not active. Note that a plot offset module is used in conjunction with this scope module for the purpose of showing all three switching waveforms in one diagram. The latter is achieved by introducing a vertical offset in the waveforms. It is instructive for the reader to repeat the simulation with active pulse centering, in which case the switch states for the first two samples of the simulation will correspond with those shown in Fig. 2.11(b). The UP-DOWN module, used in Fig. 2.24 to control the amplitude of the reference average voltage vector, may be increased from $\sqrt{3}/8 u_{DC} \rightarrow u_{DC}/\sqrt{2}$. With this setting, the modulator operates with the largest (without deforming the output waveform) possible reference incremental flux linkage amplitude, with pulse centering as was discussed in Sect. 2.4, i.e., the half-bridge reference value will remain within the supply limits $\pm u_{DC}/2$ as may be observed from this exercise.

2.6.5 Tutorial 5: Three-Phase Converter with Pulse Width Modulator

This tutorial is concerned with the implementation of a three-phase converter and modulator structure as shown in Fig. 2.9 and Fig. 2.12 respectively. The generic load $Z$ is assumed to be a 100 mH ideal inductance. The aim of this tutorial is to extend the previous tutorial activity by including a three-phase topology and modulator structure, together with a user defined average voltage reference vector. This should allow the user to examine the half-bridge voltage, load voltage, zero-sequence voltage and load current waveforms. In this example, the frequency of the rotating reference average voltage vector is (arbitrarily) set to 10 Hz, with a simulation time of 100 ms to allow visualization of one period of operation.

A simulation model of this tutorial, as given in Fig. 2.26, makes use of ideal IGBT’s and diodes, in line with the approach set out in the previous tutorials. A three-phase logic interface modules has been introduced which hold the logic modules for the half-bridge converter stages as discussed earlier for the half and full-bridge interface modules. The interface module is connected to an enable module which is used within the simulation to enable the converter at $t = 1$ ms. In the example given, the amplitude of the average voltage reference vector is determined by the product $k_U$ and $u_{DC}$, which in this case are initially chosen to be equal to $\sqrt{3}/8$ and 300 V respectively. A toggle switch is again introduced to allow the reader to enable/disable pulse centering.
Fig. 2.26 Simulation of three-phase converter with modulator

Setting the output of the toggle switch to zero disables pulse centering. Be sure to plot each time-step to observe all details.

The waveforms generated by the simulation are shown in Fig. 2.27. It is left as an exercise for the reader to reconsider the results from the simulation in the event that the factor \( k_U \) is increased to \( \frac{1}{\sqrt{2}} \) which represents the largest value that may be used, i.e., which will ensure that the absolute average voltage half-bridge reference values are less than or equal to \( \frac{u_{DC}}{2} \) when pulse centering is active. Disabling pulse centering with this value for \( k_U \) will lead to half-bridge average voltage reference values that exceed the supply window \( \pm \frac{u_{DC}}{2} \) and cannot therefore be implemented by the converter, as may be observed from this tutorial. It is particularly instructive to examine closely scope 4 during the course of the simulation because this module shows the reference vector together with the selected converter vectors used during each sample.
In practice, the simulation of comprehensive models as discussed in the previous tutorials is inhibited by the need for a relatively small computation step time. In the example above, the computation step time was set to 1 μs. Consequently, such simulations are usually slow in terms of simulation run time. An often used approach, which speeds up the simulation, is to replace the converter with three supply limited $\pm \frac{u_{DC}}{2}$ voltage sources, of which the input is derived from the half-bridge average reference generated by the pulse centering unit. The underlining concept of this approach is that the load is provided with a set of supply limited voltages which are in effect the mean (per sample) voltage generated by the modulator/converter as discussed in the previous tutorial. This tutorial aims to demonstrate this approach by removing the modulator/converter that was used in the previous tutorial and replacing the latter with a set of supply limit modules which ensures that the output is maintained within the supply voltage window $\pm \frac{u_{DC}}{2}$.

**2.6.6 Tutorial 6: Three-Phase Simplified Converter without PWM**

Fig. 2.27 Simulation results of three-phase converter with modulator
The simulation model, given in Fig. 2.28, shows how the example discussed in the previous tutorial may be adapted to this new approach. Readily identifiable in this figure are the three supply limit modules which maintain the average voltage reference values from the pulse centering module within the range $\pm \frac{u_{DC}}{2}$. The outputs of these modules can also be conveniently used to accommodate dead time effects. For this purpose, the sign of the load current must be used together with an addition gain and summation module to generate a current polarity dependent average voltage offset for each phase according to equation set (2.36). In this example, the mean half-bridge voltages are used in conjunction with a three- to two-phase (power invariant) conversion as an input to the generic model of the load. The latter is in this case an ideal inductance, which is represented by an integrator and gain $\frac{1}{L}$ module, the output of which represent the load current vector $\vec{i}$. Note also that the control of the current in the load is usually the aim of the simulation, as will become apparent in the next chapter. This implies that the need for a precise representation of the load voltage(s), other than their mean, may in most cases be avoided without comprising the purpose of the simulation.
Fig. 2.29 Simulation results of three-phase converter with pulse centering, simplified model

Some of the waveforms generated by the simulation, are shown in Fig. 2.29. A comparison of the load current waveform obtained with this and the previous tutorial shows that these are almost identical. The differences between the two are attributed to the PWM switching process which is no longer present in this simulation model. The operating conditions are otherwise identical as may be observed by comparing the average voltage reference waveforms of both simulations. The actual voltage waveforms are as expected vastly different, the average voltage per time sample $T_s$ is however identical for both tutorials. With the present choice of average voltage reference amplitude $u_{DC}/\sqrt{2}$, a circular orbit of the load vector is still possible, provided pulse centering is active. However, this choice of reference voltage amplitude is at the limit of the linear operation, which may be verified by repeating the simulation with a disabled pulse centering unit (output of toggle-switch to zero). Under these conditions, the orbit of the load voltage vector is no longer a circle, which implies that the phase waveforms are no longer sinusoidal. Note that increasing the amplitude of the reference vector beyond $u_{DC}/\sqrt{2}$ will lead to the six-step mode of operation as described towards the end of Sect. 2.4.1.
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