

Contents

- List of Symbols and Abbreviations ix
- 1 Foreword** 1
- 2 Time-to-Digital Converter Basics** 5
 - 2.1 Motivation – The Way to the Time Domain 5
 - 2.2 Analog Time-to-Digital Converters – The First Generation 8
 - 2.3 Fully Digital TDCs – The Second Generation 12
 - 2.4 Basic Digital Delay-Line Based TDC 13
 - 2.4.1 Inverter Based Time-to-Digital Converter 15
 - 2.5 Synchronous Versus Asynchronous Time Interval Measurement ... 18
- 3 Theory of TDC Operation** 19
 - 3.1 Basic Performance Figures 19
 - 3.2 Quantization Error Revisited 21
 - 3.2.1 Linear Imperfections of TDC Characteristic 22
 - 3.3 Non-Linear Imperfections of TDC Characteristic 24
 - 3.4 Dynamic Performance and Effective Resolution 25
 - 3.4.1 Basic ENOB Definition 27
 - 3.5 Timing Figures 31
 - 3.6 Noise Shaping in Time-to-Digital Converters 31
 - 3.7 Process Variations in TDCs 34
 - 3.7.1 Impact of Local Variations in Buffer Tree 36
 - 3.7.2 Impact of Local Process Variations on Delay-Line 37
 - 3.7.3 Impact of Local Process Variations on the Comparators 39
 - 3.7.4 Combined Impact of Local Variations on TDCs 40
- 4 Advanced TDC Design Issues** 43
 - 4.1 Bipolar Time-to-Digital Converter 43
 - 4.2 Looped Time-to-Digital Converter 45

4.3	Linearly Extended TDC Loop	49
4.3.1	Operation and Calibration of Linearly Extended TDC	50
4.4	Delay-Locked-Loop Based TDC	53
4.5	Hierarchical Time-to-Digital Converter	55
4.6	Multi-Event Time-to-Digital Converter	59
4.7	On-Chip Test and Characterization Engine	63
4.8	Time Domain Quantizer	65
4.9	Summary TDC Architectures	67
5	Time-to-Digital Converters with Sub-Gatedelay	
	Resolution – The Third Generation	69
5.1	Sub-Gate Delay Resolution	69
5.2	Parallel Scaled Delay Elements	70
5.2.1	Variability in TDC Based on Parallel Scaled Delay Elements	72
5.3	Vernier TDC	74
5.3.1	Vernier TDC in Loop Configuration	76
5.3.2	Variability in Vernier TDC	78
5.4	Pulse-Shrinking TDC	80
5.4.1	Pulse-Shrinking TDC in Loop Configuration	83
5.4.2	Variability in Pulse-Shrinking TDC	84
5.5	Local Passive Interpolation TDC	86
5.5.1	LPI-TDC in Loop Configuration	89
5.5.2	Resistor Sizing and Interpolation Accuracy	89
5.5.3	Variability in LPI-TDC	92
5.5.4	Implementation Example	94
5.6	Gated Ring Oscillator TDC	96
5.7	Time-to-Digital Converter with Time Amplification	98
6	Applications for Time-to-Digital Converters	103
6.1	Digital Phase Locked Loop	103
6.2	TDC Based Analog-to-Digital Converter	107
6.2.1	Dual-Slope Analog-to-Digital Converter Revisited	107
6.2.2	Pulse Position Modulation Analog-to-Digital Converter	109
6.2.3	Sigma Delta Modulator with Time Domain Quantizer	111
	References	115
	Index	119



<http://www.springer.com/978-90-481-8627-3>

Time-to-Digital Converters

Henzler, S.

2010, XII, 124 p., Hardcover

ISBN: 978-90-481-8627-3