

# Preface

Aggressive scaling of semiconductor process technology over the last several decades has resulted in creation of many new products, such as computers, camera, cell phones, and information appliances. This trend is expected to continue for the coming years and create countless opportunities and challenges. Recent developments in the semiconductor industry shows a rapid increase in interconnect frequency and design complexity. Introduction of newer technologies is now moving toward a 2-year cycle as compared to the traditional 3-year cycle. Though technology scaling helps in addressing design complexity and performance trends, it opens up a whole new spectrum of design validation challenges.

As technology scaling trend continues, interconnect parasitics play dominant role in determining chip performance and functionality. Interconnect delay becomes a significant portion of chip delay and noise/crosstalk caused due to parasitic coupling poses threat to circuit functionality. With increasing demands for high signal speeds coupled with reduced feature sizes, interconnect effects such as signal delay, distortion, and crosstalk become the dominant factors limiting overall performance of high-speed systems. If not considered during the design stage, interconnect effects can cause failed designs.

Advancement of VLSI technology leads to the development of high-speed complex integrated circuits (ICs) in deep submicron and nanoscale regime. Due to shrinking feature size and increasing clock frequency, interconnect plays an important role in determining the overall chip performance. In current scenario, interconnect delay dominates over gate delay. Depending on the length, interconnects can be classified to local, semi-global, and global interconnects. With ever-increasing lengths, global interconnects are prone to large interconnect delays, signal integrity issues, and higher current densities. The global interconnects are widely employed to distribute data, clock, power supply, and ground throughout the entire chip. At global level of interconnects, most of the conventional materials (such as Al or Cu) are susceptible to electromigration due to high current density. This electromigration problem substantially affects the reliability of high-speed circuits. To avoid such problems, researchers are forced to find an alternative solution.

Carbon nanotubes (CNTs) can be considered as an alternative interconnect material for current nanoscale technologies. After discovery in 1991, CNTs have received tremendous research interest for their unique mechanical, electrical, thermal, and chemical properties. The  $sp^2$  bonding in graphene is even stronger than the  $sp^3$  bonds in diamond that gives CNTs very high mechanical strength. The unique electrical and thermal properties are mainly due to movement of electrons in one-dimension (1D). Due to 1D movement, electrons can be scattered only in backward direction. Mean free path ( $mfp$ ) in high quality nanotubes is in the range of micrometers. This is in contrast to a three-dimensional (3D) metallic wire wherein electrons can be backscattered by a series of small angle scatterings, and therefore  $mfps$  are in the range of a few tens of nanometers. Due to long  $mfp$ , the ballistic phenomenon can be observed in CNTs that is responsible for its outstanding electrical and thermal behavior. Moreover, an isolated CNT can carry current density in excess of  $10^9$  A/cm<sup>2</sup>, which can enhance the electrical performance as well as eliminate electromigration reliability concerns that plagues current nanoscale Cu interconnects.

This book primarily focuses on the performance analysis of CNT based interconnects in current research scenario. Different CNT structures are modeled on basis of transmission line theory. Performance comparison for different CNT structures illustrates that CNTs are more promising than Cu or other materials used in global VLSI interconnects. The organization of the book chapters is as follows: Chapter 1 provides an overview of current research scenario and basics of interconnects. Unique crystal arrangements and the physical properties of CNTs are described in Chap. 2. Furthermore, this chapter illustrates the production, purification, and applications of CNTs. Chapter 3 provides a brief review of the research work carried out in the area of CNT interconnect modeling. The geometry and equivalent  $RLC$  parameters for different single and bundled CNTs are also discussed in this chapter. A comparative analysis of crosstalk and delay for different single and bundled CNT structures is carried out in Chap. 4. Finally, Chap. 5 introduces unique mixed CNT bundle structures and their equivalent electrical models.

We would like to express our sincere gratitude to Mr. Arsalan Alam, Mr. Madimatla Satyanarayana Murthy and Mr. Nisarg D. Pandya for their unrestrained help in successful completion of this book. We also acknowledge for the help rendered by all the research scholars and faculty members of Microelectronics and VLSI group, Indian Institute of Technology Roorkee for constructive technical discussions at various stages of preparation of this book.

Brajesh Kumar Kaushik  
Manoj Kumar Majumder



<http://www.springer.com/978-81-322-2046-6>

Carbon Nanotube Based VLSI Interconnects  
Analysis and Design

Kaushik, B.K.; Majumder, M.K.

2015, XI, 86 p. 57 illus., Softcover

ISBN: 978-81-322-2046-6