

# Contents

<b>1</b>	<b>Introduction</b> .....	1
1.1	Introduction.....	1
1.2	Historical Background [1].....	2
1.3	Why Low Power? [2].....	7
1.4	Sources of Power Dissipations [3].....	9
1.4.1	Dynamic Power.....	10
1.4.2	Static Power.....	13
1.5	Low-Power Design Methodologies.....	14
1.6	Chapter Summary.....	16
1.7	Review Questions.....	16
	References.....	17
<b>2</b>	<b>MOS Fabrication Technology</b> .....	19
2.1	Introduction.....	19
2.2	Basic Fabrication Processes [1, 2].....	20
2.2.1	Wafer Fabrication.....	20
2.2.2	Oxidation.....	20
2.2.3	Mask Generation.....	21
2.2.4	Photolithography.....	22
2.2.5	Diffusion.....	23
2.2.6	Deposition.....	24
2.3	nMOS Fabrication Steps [2, 3].....	24
2.4	CMOS Fabrication Steps [2, 3].....	26
2.4.1	The n-Well Process.....	26
2.4.2	The p-Well Process.....	30
2.4.3	Twin-Tub Process.....	31
2.5	Latch-Up Problem and Its Prevention.....	31
2.5.1	Use of Guard Rings.....	33
2.5.2	Use of Trenches.....	34
2.6	Short-Channel Effects [6].....	34
2.6.1	Channel Length Modulation Effect.....	35

2.6.2	Drain-Induced Barrier Lowering.....	35
2.6.3	Channel Punch Through.....	36
2.7	Emerging Technologies for Low Power.....	37
2.7.1	Hi-K Gate Dielectric.....	37
2.7.2	Lightly Doped Drain–Source.....	38
2.7.3	Silicon on Insulator.....	39
2.7.4	Advantages of SOI.....	40
2.7.5	FinFET.....	40
2.8	Chapter Summary.....	41
2.9	Review Questions.....	41
	References.....	42
<b>3</b>	<b>MOS Transistors</b> .....	<b>43</b>
3.1	Introduction.....	43
3.2	The Structure of MOS Transistors.....	44
3.3	The Fluid Model.....	45
3.3.1	The MOS Capacitor.....	46
3.3.2	The MOS Transistor.....	47
3.4	Modes of Operation of MOS Transistors [2].....	50
3.5	Electrical Characteristics of MOS Transistors.....	50
3.5.1	Threshold Voltage.....	54
3.5.2	Transistor Transconductance $g_m$ .....	56
3.5.3	Figure of Merit.....	57
3.5.4	Body Effect.....	57
3.5.5	Channel-Length Modulation.....	58
3.6	MOS Transistors as a Switch [3].....	60
3.6.1	Transmission Gate.....	60
3.7	Chapter Summary.....	64
3.8	Review Questions.....	64
	References.....	65
<b>4</b>	<b>MOS Inverters</b> .....	<b>67</b>
4.1	Introduction.....	67
4.2	Inverter and Its Characteristics.....	68
4.3	MOS Inverter Configurations.....	70
4.3.1	Passive Resistive as Pull-up Device.....	71
4.3.2	nMOS Depletion-Mode Transistor as Pull up.....	72
4.3.3	nMOS Enhancement-Mode Transistor as Pull up.....	74
4.3.4	The pMOS Transistor as Pull Up.....	75
4.3.5	pMOS Transistor as a Pull Up in Complementary Mode.....	76
4.3.6	Comparison of the Inverters.....	82
4.4	Inverter Ratio in Different Situations.....	82
4.4.1	An nMOS Inverter Driven by Another Inverter.....	83
4.4.2	An nMOS Inverter Driven Through Pass Transistors.....	84

4.5	Switching Characteristics.....	86
4.5.1	Delay-Time Estimation .....	87
4.5.2	Ring Oscillator .....	89
4.6	Delay Parameters .....	90
4.6.1	Resistance Estimation .....	91
4.6.2	Area Capacitance of Different Layers.....	92
4.6.3	Standard Unit of Capacitance $C_g$ .....	93
4.6.4	The Delay Unit .....	94
4.7	Driving Large Capacitive Loads .....	94
4.7.1	Super Buffers.....	95
4.7.2	BiCMOS Inverters .....	97
4.7.3	Buffer Sizing .....	98
4.8	Chapter Summary.....	100
4.9	Review Questions.....	100
	References .....	102
<b>5</b>	<b>MOS Combinational Circuits.....</b>	<b>103</b>
5.1	Introduction.....	103
5.2	Pass-Transistor Logic.....	104
5.2.1	Realizing Pass-Transistor Logic.....	105
5.2.2	Advantages and Disadvantages.....	107
5.2.3	Pass-Transistor Logic Families .....	109
5.3	Gate Logic.....	113
5.3.1	Fan-In and Fan-Out.....	113
5.3.2	nMOS NAND and NOR Gates .....	114
5.3.3	CMOS Realization .....	115
5.3.4	Switching Characteristics.....	117
5.3.5	CMOS NOR Gate .....	119
5.3.6	CMOS Complex Logic Gates .....	119
5.4	MOS Dynamic Circuits.....	120
5.4.1	Single-Phase Dynamic Circuits.....	121
5.4.2	Two-Phase Dynamic Circuits.....	122
5.4.3	CMOS Dynamic Circuits .....	123
5.4.4	Advantages and Disadvantages .....	125
5.4.5	Domino CMOS Circuits.....	128
5.4.6	NORA Logic .....	129
5.5	Some Examples.....	130
5.6	Chapter Summary.....	135
5.7	Review Questions.....	137
	References .....	139
<b>6</b>	<b>Sources of Power Dissipation .....</b>	<b>141</b>
6.1	Introduction.....	141
6.2	Short-Circuit Power Dissipation [1].....	143

- 6.3 Switching Power Dissipation [1] ..... 147
  - 6.3.1 Dynamic Power for a Complex Gate ..... 149
  - 6.3.2 Reduced Voltage Swing ..... 149
  - 6.3.3 Internal Node Power ..... 150
  - 6.3.4 Switching Activity [2, 3]..... 150
  - 6.3.5 Switching Activity of Static CMOS Gates..... 151
  - 6.3.6 Inputs Not Equiprobable ..... 152
  - 6.3.7 Mutually Dependent Inputs..... 152
  - 6.3.8 Transition Probability in Dynamic Gates..... 155
  - 6.3.9 Power Dissipation due to Charge Sharing..... 156
- 6.4 Glitching Power Dissipation ..... 157
- 6.5 Leakage Power Dissipation [4] ..... 158
  - 6.5.1 p–n Junction Reverse-Biased Current..... 158
  - 6.5.2 Band-to-Band Tunneling Current..... 160
  - 6.5.3 Subthreshold Leakage Current..... 160
- 6.6 Conclusion..... 171
- 6.7 Chapter Summary..... 172
- 6.8 Review Questions..... 172
- References ..... 173
  
- 7 Supply Voltage Scaling for Low Power ..... 175**
  - 7.1 Introduction..... 175
  - 7.2 Device Feature Size Scaling [1]..... 178
    - 7.2.1 Constant-Field Scaling..... 178
    - 7.2.2 Constant-Voltage Scaling..... 181
    - 7.2.3 Short-Channel Effects ..... 182
  - 7.3 Architectural-Level Approaches..... 183
    - 7.3.1 Parallelism for Low Power..... 183
    - 7.3.2 Multi-Core for Low Power..... 186
    - 7.3.3 Pipelining for Low Power ..... 187
    - 7.3.4 Combining Parallelism with Pipelining ..... 188
  - 7.4 Voltage Scaling Using High-Level Transformations ..... 189
  - 7.5 Multilevel Voltage Scaling ..... 192
  - 7.6 Challenges in MVS ..... 194
    - 7.6.1 Voltage Scaling Interfaces..... 195
    - 7.6.2 Converter Placement ..... 196
    - 7.6.3 Floor Planning, Routing, and Placement..... 197
    - 7.6.4 Static Timing Analysis ..... 197
    - 7.6.5 Power-Up and Power-Down Sequencing..... 197
    - 7.6.6 Clock Distribution..... 198
    - 7.6.7 Low-Voltage Swing..... 198
  - 7.7 Dynamic Voltage and Frequency Scaling ..... 199
    - 7.7.1 Basic Approach ..... 199
    - 7.7.2 DVFS with Varying Work Load..... 202
    - 7.7.3 The Model ..... 204

7.7.4	Workload Prediction.....	205
7.7.5	Discrete Processing Rate.....	206
7.7.6	Latency Overhead.....	207
7.8	Adaptive Voltage Scaling.....	208
7.9	Subthreshold Logic Circuits.....	209
7.10	Chapter Summary.....	210
7.11	Review Questions.....	211
	References.....	212
<b>8</b>	<b>Switched Capacitance Minimization.....</b>	<b>213</b>
8.1	Introduction.....	213
8.2	System-Level Approach: Hardware–Software Codesign.....	214
8.3	Transmeta’s Crusoe Processor.....	215
8.3.1	The Hardware.....	216
8.3.2	The Software.....	217
8.4	Bus Encoding.....	220
8.4.1	Gray Coding.....	221
8.4.2	One-Hot Coding.....	223
8.4.3	Bus-Inversion Coding.....	224
8.4.4	T0 Coding.....	224
8.5	Clock Gating.....	226
8.5.1	CG Circuits.....	227
8.5.2	CG Granularity.....	229
8.6	Gated-Clock FSMs.....	231
8.7	FSM State Encoding.....	233
8.8	FSM Partitioning.....	234
8.9	Operand Isolation.....	235
8.10	Precomputation.....	236
8.11	Glitching Power Minimization.....	237
8.12	Logic Styles for Low Power.....	238
8.12.1	Static CMOS Logic.....	239
8.12.2	Dynamic CMOS Logic.....	240
8.12.3	PTL.....	242
8.12.4	Synthesis of Dynamic CMOS Circuits.....	243
8.12.5	Synthesis of PTL Circuits.....	248
8.12.6	Implementation and Experimental Results.....	250
8.13	Some Related Techniques for Dynamic Power Reduction.....	254
8.14	Chapter Summary.....	256
8.15	Review Questions.....	257
	References.....	258
<b>9</b>	<b>Leakage Power Minimization.....</b>	<b>261</b>
9.1	Introduction.....	261
9.2	Fabrication of Multiple Threshold Voltages.....	263
9.2.1	Multiple Channel Doping.....	263

- 9.2.2 Multiple Oxide CMOS ..... 264
- 9.2.3 Multiple Channel Length ..... 265
- 9.2.4 Multiple Body Bias ..... 266
- 9.3 VTCMOS Approach..... 266
- 9.4 Transistor Stacking..... 267
- 9.5 MTCMOS Approach..... 270
- 9.6 Power Gating [8]..... 272
  - 9.6.1 Clock Gating Versus Power Gating..... 272
  - 9.6.2 Power-Gating Issues..... 273
- 9.7 Isolation Strategy ..... 278
- 9.8 State Retention Strategy..... 281
- 9.9 Power-Gating Controller..... 282
- 9.10 Power Management..... 284
  - 9.10.1 Combining DVFS and Power Management..... 285
- 9.11 Dual- $V_t$  Assignment Approach (DTCMOS) [10]..... 286
- 9.12 Delay-Constrained Dual- $V_t$  CMOS Circuits [12]..... 289
- 9.13 Energy-Constrained Dual- $V_t$  CMOS Circuits[13]..... 293
- 9.14 Dynamic  $V_{th}$  Scaling ..... 298
- 9.15 Chapter Summary..... 299
- 9.16 Review Questions..... 300
- References ..... 301
  
- 10 Adiabatic Logic Circuits ..... 303**
  - 10.1 Introduction..... 303
  - 10.2 Adiabatic Charging..... 304
  - 10.3 Adiabatic Amplification ..... 306
  - 10.4 Adiabatic Logic Gates ..... 307
  - 10.5 Pulsed Power Supply..... 308
  - 10.6 Stepwise Charging Circuits..... 310
    - 10.6.1 Stepwise Driver Using Tank Capacitors ..... 313
  - 10.7 Partially Adiabatic Circuits ..... 313
    - 10.7.1 Efficient Charge Recovery Logic..... 314
    - 10.7.2 Positive Feedback Adiabatic Logic Circuits ..... 315
    - 10.7.3 2N–2N2P Inverter/Buffer..... 316
  - 10.8 Some Important Issues ..... 316
  - 10.9 Chapter Summary..... 320
  - 10.10 Review Questions..... 320
  - References ..... 321
  
- 11 Battery-Aware Systems ..... 323**
  - 11.1 Introduction ..... 323
  - 11.2 The Widening Battery Gap [1] ..... 324
  - 11.3 Overview of Battery Technologies..... 326
    - 11.3.1 Nickel Cadmium ..... 326
    - 11.3.2 Nickel–Metal Hydride..... 327

- 11.3.3 Lithium Ion..... 328
- 11.3.4 Rechargeable Alkaline..... 329
- 11.3.5 Li Polymer..... 329
- 11.4 Battery Characteristics [4, 5]..... 329
  - 11.4.1 Rate Capacity Effect..... 330
  - 11.4.2 Recovery Effect..... 331
  - 11.4.3 Memory Effect ..... 331
  - 11.4.4 Usage Pattern..... 331
  - 11.4.5 Battery Age..... 332
- 11.5 Principles of Battery Discharge..... 332
- 11.6 Battery Modeling..... 333
- 11.7 Battery-Driven System Design..... 335
  - 11.7.1 Multi-battery System..... 336
  - 11.7.2 Battery-Aware Task Scheduling..... 336
  - 11.7.3 Task Scheduling with Voltage Scaling [12]..... 339
- 11.8 Wireless Sensor Networks..... 340
- 11.9 Energy-Aware Routing..... 346
- 11.10 Assisted-LEACH..... 348
- 11.11 Conclusion..... 352
- 11.12 Chapter Summary..... 353
- 11.13 Review Questions..... 353
- References..... 354
  
- 12 Low-Power Software Approaches ..... 355**
  - 12.1 Introduction..... 355
  - 12.2 The Hardware..... 356
  - 12.3 Machine-Independent Software Optimizations..... 359
    - 12.3.1 Compilation For Low Power..... 359
  - 12.4 Combining Loop Optimizations with DVFS ..... 364
    - 12.4.1 Loop Unrolling..... 365
    - 12.4.2 Loop Tiling..... 366
    - 12.4.3 Loop Permutation..... 367
    - 12.4.4 Strength Reduction..... 367
    - 12.4.5 Loop Fusion ..... 368
    - 12.4.6 Loop Peeling ..... 369
    - 12.4.7 Loop Unswitching..... 370
  - 12.5 Power-Aware Software Prefetching ..... 371
    - 12.5.1 Compilation For Low Power..... 375
    - 12.5.2 Experimental Methodology and Results..... 380
    - 12.5.3 Conclusions..... 384
  - 12.6 Chapter Summary..... 384
  - 12.7 Review Questions..... 385
  - References..... 385
  
- Index..... 387**



<http://www.springer.com/978-81-322-1936-1>

Low-Power VLSI Circuits and Systems

Pal, A.

2015, XXXVII, 389 p. 303 illus., Hardcover

ISBN: 978-81-322-1936-1