Guest Editors' Preface
Special Issue on Reversible Computing

Reversible computing is emerging as a promising computing paradigm with applications in ultra-low power green computing and emerging nanotechnologies such as quantum computing, quantum dot cellular automata (QCA), optical, etc. Reversible circuits are similar to conventional logic circuits except that they are built from reversible gates. In reversible gates, there is a unique, one-to-one mapping between the inputs and outputs, not the case with conventional logic. In this special issue on reversible computing, articles are selected on physical realizations, experimental validations, and theoretical solutions of reversible computing in conventional CMOS paradigms as well as in emerging computing paradigms such as optical computing, etc. Also, the papers are selected on topics of special interest such as reversible circuit and logic synthesis, quantum circuit description language, and reversible basic linear algebra subprograms. This special issue consists of eight papers and is aimed at educators, researchers, and students who are engaged in reversible computing research and education.

The papers are arranged as follows:

The first paper, entitled "Adiabatic CMOS: Limits of Reversible Energy Recovery and First Steps for Design Automation," by Ismo Hänninen, Gregory L. Snider, and Craig S. Lent proposes to implement adiabatic CMOS circuits utilizing split-level rails and Bennett clocking, which enable energy-recovery in standard CMOS logic gates with only minor modifications. Also, it outlines an approach to integrate the automatic generation of the adiabatic circuits into the standard circuit design flow, including standard gate logic synthesis and place-and-route.

The second paper, entitled "Ultrafast All-Optical Reversible Peres and Feynman-Double Logic Gates with Silicon Microring Resonators," by Purnima Sethi and Sukhdev Roy, presents designs of reversible Peres logic gate and Feynman-Double logic gate based on all-optical switching by two-photon absorption-induced free-carrier injection in silicon add-drop microring resonators.

The third paper, entitled "Design of Reversible Adder-Subtractor and its Mapping in Optical Computing Domain," by Saurabh Kotiyal, Himanshu Thapliyal, and Nagarajan Ranganathan presents the optical implementation of an n bit reversible ripple carry adder. The optical reversible adder design is based on two new optical reversible gates referred to as optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) and the existing optical Feynman gate. The design methodologies to design a reversible adder-subtractor that is controlled by the control signal to perform addition or subtraction operation are also presented.

Making applications reversible by relying on computation rather than on memory is ideal for large-scale parallel computing, especially for the next generation of supercomputers in which memory is expensive in terms of latency, energy, and price. In this direction the fourth paper, entitled "Towards Reversible Basic Linear Algebra

Subprograms: A Performance Study," by Kalyan S. Perumalla and Srikanth B. Yoginath presents a new Reversible BLAS (RBLAS) library interface, and a prototype has been implemented with two modes: (1) a memory-mode in which reversibility is obtained by checkpointing to memory and (2) a computational-mode in which nothing is saved, and restoration is done entirely via inverse computation.

The fifth paper, entitled "Synthesis and Optimization by Quantum Circuit Description Language," by Mariam Zomorodi-Moghadam, Mohammad-Amin Taherkhani, and Keivan Navi describes the infrastructure of synthesizing quantum circuits via a quantum description language. A new quantum circuit description language named QCDL is introduced which comprises instructions for quantum unitary operations and high-level structures which are synthesized into quantum logic level architecture.

The sixth paper, entitled "An Approach to Reversible Logic Synthesis Using Input and Output Permutations," by Kamalika Datta, Indranil Sengupta, Hafizur Rahaman, and Rolf Drechsler presents two alternate methods for reordering the variables so as to reduce the cost of synthesized circuit. In the first method, a fast Evolutionary Algorithm (EA) is used to search for an output permutation based on a properly chosen cost function. In the second method, using the notion of encoded truth table, a Simulated Annealing (SA)-based approach is used to search for both input and output permutations in an integrated fashion.

The seventh paper, entitled "Synthesis of Reversible Circuits Based on EXORs of Products of EXORs," by Linh Tran, Ben Schaeffer, Addison Gronquist, Marek Perkowski, and Pawel Kerntopf introduces a new concept of reversible circuits based on EXOR-sum of Products-of-EXOR-sums (EPOE). Two algorithms are introduced that synthesize reversible functions using these new EPOE structures. The motivation for this work is to reduce the number of multiple controlled Toffoli gates and their number of inputs.

The eighth paper, entitled "Improved Cube List Based Cube Pairing Approach for Synthesis of ESOP Based Reversible Logic," by Chandan Bandyopadhyay, Hafizur Rahaman, and Rolf Drechsler presents an approach for generating improved ESOP cubes and then pairing the cubes to implement enhanced Toffoli network. The improved cube list generation method differs from other earlier approaches in the sense that in the proposed technique, the improved ESOP cubes have been constructed without using any existing tool.

We would like to thank all the authors for their valuable contribution to this special issue. We would like to acknowledge and thank the reviewers for their valuable and timely efforts to ensure the high quality of the papers. We also like to thank Editor-in-Chief of Springer's LNCS Transactions on Computational Science, Marina L. Gavrilova, University of Calgary, Canada, for her wonderful support and providing the opportunity to organize this special issue. We hope that the special issue on reversible computing will serve as a valuable resource for the reversible computing community.

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