Preface

The phenomenal increases in computer system performance in recent years have been accompanied by a commensurate increase in power and energy dissipation. The latter has directly resulted in demand for expensive packaging and cooling technology, an increase in product cost, and a decrease in product reliability in all segments of the computing market. Moreover, the higher power/energy dissipation has significantly reduced battery life in portable systems. While system designers have traditionally relied on circuit-level techniques to reduce power/energy, there is a growing need to address power/energy dissipation at all levels of the computer system.

We are pleased to welcome you to the proceedings of the Power-Aware Computer Systems (PACS 2000) workshop. PACS 2000 was the first workshop in its series and its aim was to bring together experts from academia and industry to address power-/energy-awareness at all levels of computer systems. In these proceedings, we bring you several excellent research contributions spanning a wide spectrum of areas in power-aware systems, from application all the way to compilers and microarchitecture, and to power/performance estimating models and tools. We have grouped the contributions into the following specific categories: (1) power-aware microarchitectural/circuit techniques, (2) application/compiler power optimizations, (3) exploiting opportunity for power optimization in instruction scheduling and cache memories, and (4) power/performance models and tools.

The first and third group of papers primarily address the opportunity for power optimization at the architectural/microarchitectural level. While there are large variabilities in hardware resource utilization within and across applications, high-performance processor cores are designed for worst-case resource demands and therefore often waste power/energy while idling. The papers in these groups propose techniques to take advantage of the variability in resource demand. These include resizing instruction issue queue, dynamically varying the instruction issue width, supply-gating inactive cache block frames to reduce leakage power/energy dissipation, mechanisms to trigger dynamical voltage scaling, and predicting functional unit activation time to reduce inductive noise during the on/off transition.

The second group of papers focus on application transformations and compiler optimization techniques to reduce energy/power. The papers propose energy-efficient dynamic memory allocation schemes for an MPEG multimedia player, power-aware graphics rendering algorithms and hardware to exploit content variation and human visual perception, and compiler optimization to estimate memory-intensive program phases that can trigger dynamic voltage scaling to slow down the processor clock.

The last group of papers present power/performance estimation models for high-end microprocessors. The first paper presents a tool from Intel that inte-

grates both analytical models and empirical data for power estimation with SimpleScalar, a cycle-accurate performance estimator. The second paper describes two simulation models from IBM to evaluate power/performance characteristics of PowerPC processors. The models trade off accuracy for speed. The third paper compares and contrasts the effectiveness and merits of two existing tools for power/performance estimation.

PACS 2000 was a highly successful forum, thanks to a number of high-quality submissions, the enormous efforts of the program committee, the keynote speaker, and the attendees. We would like to thank Shekhar Borkar for preparing the keynote speech, pinpointing the technological scaling trends and their impact on energy/power consumption in general and the increase in transistor subthreshold leakage current in particular. We would like to thank Konrad Lai for the excellent keynote delivery on behalf of Shekhar, and accepting to substitute for Shekhar on short notice, due to an emergency. We would like to thank Larry Rudolf, James Hoe, and Boon Ang and the other members of the ASPLOS-IX organizing committee who publicized the workshop and helped with local accommodation.

May 2001 Babak Falsafi and T. N. Vijaykumar

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