Preface

With the advances in the scale and complexity of modern integrated circuits (ICs), Simulation Program with Integrated Circuit Emphasis (SPICE) based circuit simulators are facing performance challenges, especially for post-layout simulations. Advances in semiconductor technologies have greatly promoted the development of parallel computers, and, hence, parallelization has become a promising approach to accelerate circuit simulations. Parallel circuit simulation has been a popular research topic for a few decades since the invention of SPICE. The sparse direct solver implemented by sparse lower–upper (LU) factorization is the biggest bottleneck in modern full SPICE-accurate IC simulations, since it is extremely difficult to parallelize. This is a practical challenge which both academia and industry are facing.

This book describes algorithmic methods and parallelization techniques that aim to realize a parallel sparse direct solver named NICSLU (NICS is short for Nano-Scale Integrated Circuits and Systems, the name of our laboratory in Tsinghua University), which is specially targeted at SPICE-like circuit simulation problems. We propose innovative numerical algorithms and parallelization framework for designing NICSLU. We describe a complete flow and detailed parallel algorithms of NICSLU. We also show how to improve the performance of NICSLU by developing novel numerical techniques. NICSLU can be applied to any SPICE-like circuit simulators and has been proven to be high performance by actual circuit simulation applications.

There are eight chapters in this book. Chapter 1 gives a general introduction to SPICE-like circuit simulation and also describes the challenges of parallel circuit simulation. Chapter 2 comprehensively reviews existing work on parallel circuit simulation techniques, including various software algorithms and hardware acceleration techniques. Chapter 3 covers the overall flow and all the core steps of NICSLU.

Starting from Chap. 4, we present the proposed algorithmic methods and parallelization techniques of NICSLU in detail. We will describe two parallel factorization algorithms, a full factorization with partial pivoting and a re-factorization without partial pivoting, based on an innovative parallelization framework. The two algorithms are both compatible with SPICE-like circuit simulation applications.

Three improvement techniques are presented in Chap. 5 to further enhance the performance of NICSLU. Test results of NICSLU, including benchmark results and circuit simulation results, are presented and analyzed in Chap. 6.

In Chap. 7, we present a graph-based performance model to evaluate the performance and find the bottlenecks of NICSLU. This model is expected to help readers understand the performance of NICSLU in more depth, and, thus, potentially find further improvement points.

Chapter 8 concludes the book by summarizing the proposed innovative techniques and discussing possible future research directions.

To better understand the algorithms and parallelization techniques presented in this book, readers can download the source code of an old version of NICSLU from http://nics.ee.tsinghua.edu.cn/people/chenxm/nicslu.htm.

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