Chapter 2
The Chopping Technique

As briefly explained in Chap. 1, the chopping technique has been applied to convert DC input signals into AC signals that can then be capacitively coupled to the input stage of a capacitively coupled amplifier. Since chopping up-modulates offset and $1/f$ noise away from DC, high precision, i.e., microvolt offset and low $1/f$ noise, can be achieved. These characteristics make such amplifiers ideally suited for the amplification of small low-frequency signals. In this chapter, the basic working principle of chopping and its application in precision amplifiers will be discussed. It will be shown that chopping usually results in AC ripple at the chopping frequency, which must then be suppressed. Thus, the techniques to reduce this ripple will also be described. After this, the non-idealities of chopping will be discussed, followed by a summary of its pros and cons. Finally, conclusions will be drawn at the end of the chapter.

2.1 Basic Working Principle

Chopping involves the use of two synchronized polarity-reversing choppers [1–4] for precise modulation and demodulation. Each chopper consists of four switches driven by clock signals with two complementary phases at a certain chopping frequency (f_{chop}). In CMOS technology, the switches can be simply implemented by MOSFETs, as shown in Fig. 2.1. In the time domain, as shown in Fig. 2.2, the input chopper converts an input DC signal into a square wave. After amplification, the output chopper demodulates this square wave back to DC. In the frequency domain, the input chopper moves the DC signal to the odd harmonics of f_{chop}, and the output chopper moves the high-frequency components back to DC.
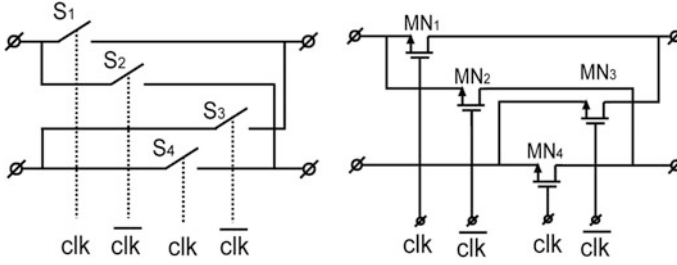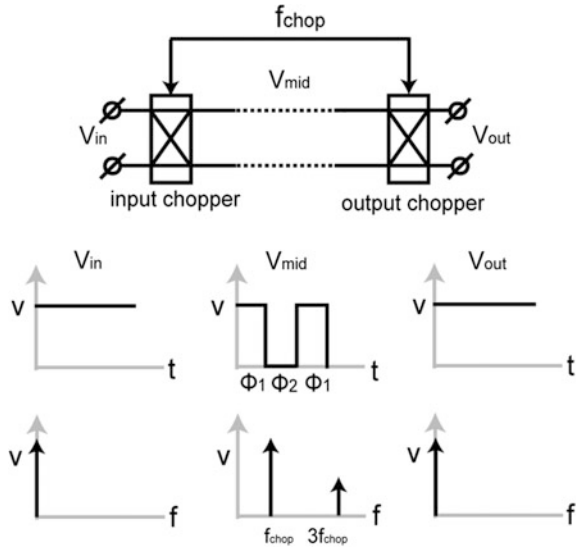
Fig. 2.1 Schematic of a chopper and its implementation with NMOS transistors

Fig. 2.2 Working principle
of two synchronized choppers

2.2   Basic Chopper Amplifier Topologies

2.2.1   Basic Chopper Opamp and Instrumentation Amplifier Topologies

When chopping is applied to an opamp, as shown in Fig. 2.3, the input signal is first moved to the odd harmonics of f_{chop} by CH_{in}, then amplified, and finally moved back to DC. Meanwhile, the offset and $1/f$ noise of G_{m1} are up-modulated by CH_{out} to the odd harmonics of f_{chop}. Thus, ideally, an offset- and $1/f$ noise-free opamp is obtained. It is worth pointing out that in Fig. 2.3, the effective DC gain of the opamp is equal to the gain of G_{m1} at f_{chop}, which is usually much lower than its gain at DC. Thus, to ensure sufficient gain, multiple gain stages are often employed [5]. In a two-stage opamp, for instance, the output chopper (CH_{out}) can be located at the

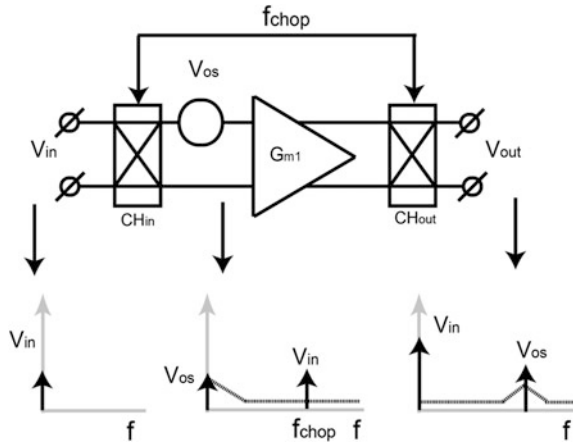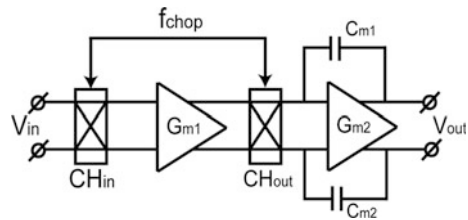**Fig. 2.3** Voltages in the frequency domain in a chopper amplifier

Fig. 2.4 Schematic of a two-stage chopper opamp

input of the second stage, as shown in Fig. 2.4. The amplifier's effective DC gain is then the gain of G_{m1} at f_{chop} multiplied by the DC gain of G_{m2}.

Chopping usually does not introduce extra noise, especially when the choppers are positioned at low impedance nodes. In the situation of Fig. 2.4, for instance, the main noise source is the on-resistance of the input chopper. Thus, by making this low enough, its noise contribution can be made negligible.

To realize a chopper instrumentation amplifier (IA), a resistive feedback network can be added around a chopper opamp (Fig. 2.5). If high-input impedance is

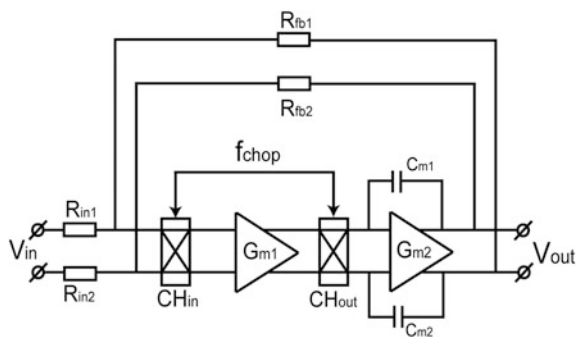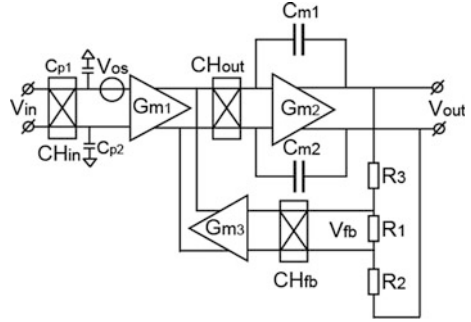**Fig. 2.5** Schematic of chopper IA with resistive feedback network

required, an extra feedback transconductance G_{m3} can be employed together with a
resistive divider (Fig. 2.6). The latter topology is known as an indirect current
feedback IA (CFIA) [1, 3]. The high-open-loop gain of the opamp ensures that the
output current of G_{m1} cancels that of G_{m3}, so that V_{in} is equal to V_{fb}. Thus, V_{out} will
be equal to $V_{in} \times \frac{G_{m1}}{G_{m3}} \times \frac{R_1 + R_2 + R_3}{R_1}$. In this case, G_{m3} also introduces offset and
$1/f$ noise; thus, a third chopper CH_{fb} must be employed.

The up-modulated offset and $1/f$ noise in both chopper opamps and IAs, how-
ever, will appear as output ripple which must then be eliminated. A straightforward
way of doing this is by employing a low-pass filter at the output of the amplifier.
However, the filter itself can introduce extra offset (in the case of an active filter)
and noise (both for active and for passive filters), which are only suppressed by the
closed-loop gain of the previous chopper amplifier and, thus, may not be suffi-
ciently reduced [6]. Moreover, to obtain sufficient filtering, the cutoff frequency of
the filter should be sufficiently low, which also limits the bandwidth of the whole
signal path (chopper amplifier + filter). Thus, alternative ripple-reduction tech-
niques are required.

The chopper stabilization technique is one way to suppress chopper ripple while
not necessarily introducing extra offset and $1/f$ noise, and affecting the signal
bandwidth. It involves placing a chopper amplifier in an auxiliary signal path,
which then does not limit the bandwidth of a main amplifier. By limiting the
bandwidth of the auxiliary single path, its ripple is reduced. In the following, the
chopper stabilization technique will be discussed in more detail.

2.2.2   Chopper Stabilization

The basic topology of a chopper-stabilized amplifier is shown in Fig. 2.7 [1, 3, 7].
The amplifier consists of two signal paths: a main signal path consisting of A_1 and
an auxiliary signal path consisting of A_2 and A_3. This topology has been used in
several state-of-the-art designs [7–10]. The main signal path provides wide signal

Fig. 2.7 Block diagram of a chopper-stabilized amplifier with negative feedback network
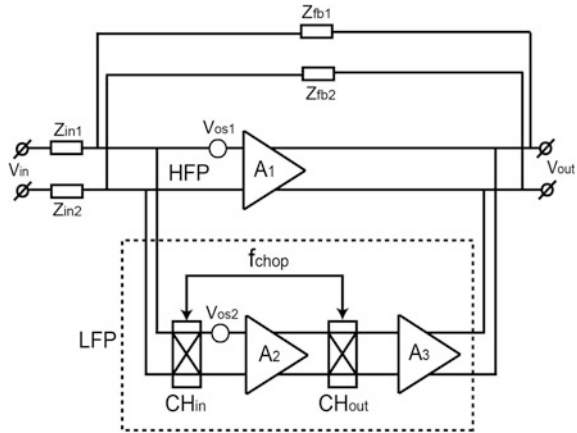
bandwidth and is thus often referred to as the high-frequency path (HFP), while the auxiliary path provides low offset and high DC gain, usually has limited bandwidth, and thus is often called as the low-frequency path (LFP). To achieve low offset, the offset of the HFP must be taken care of. In the presence of a global negative feedback as shown in Fig. 2.7, the offset of A_1 (V_{os1}) will be amplified and then fed back to the input of the LFP. Thus, it will be corrected by the high-gain LFP. The residual offset due to V_{os1} can be expressed as [3]:

$$V_{error} = \frac{V_{os1} \times A_1}{A_2 \times A_3}. \tag{2.1}$$

Thus, as long as there is sufficient gain in the LFP, the residual offset is negligible. It is worth mentioning that the low-frequency $1/f$ noise of the HFP is also suppressed by the LFP in the same manner. The offset of the LFP, however, is removed by chopping.

The main advantage of chopper stabilization is that it can achieve high bandwidth and high DC accuracy at the same time. The chopping ripple generated in the LFP is suppressed by limiting its bandwidth, e.g., by the deliberate insertion of a low-pass filter (often an integrator). The disadvantage of this approach, however, is the reduction in power efficiency associated with the use of two signal paths. Another potential concern is that when microvolt-level residual ripple is required, a low-pass filter requiring large passive components may be needed to restrict the bandwidth of the LFP. This can increase the chip area significantly. Thus, better methods to sufficiently reduce the chopping ripple without consuming too much power and chip area are required.

2.3   Ripple-Reduction Techniques

Consider the case of the CFIA shown in Fig. 2.6, and if its bandwidth is lower than the chopping frequency, then the ripple voltage V_{ripple} at its output will be a triangular wave and its amplitude can be estimated by:

$$V_{ripple} = \frac{V_{os} \times G_{m1}}{2 \times f_{chop} \times C_{m1,2}}, \tag{2.2}$$

where V_{os} is the offset of G_{m1}. For instance, with V_{os} = 5 mV, G_{m1} = 100 μS, $C_{m1,2}$ = 10 pF, and f_{chop} = 50 kHz, V_{ripple} is 0.5 V. Such a large ripple is usually not tolerable and must be removed. To suppress a 0.5 V ripple to, for instance, 50 μV, a suppression factor of 10,000 is needed. This cannot be easily achieved by either employing a low-pass filter at the output of the amplifier or chopper stabilization.

Recently, many highly effective ripple-reduction techniques have been published [4, 5, 7–15]. Four of these will be discussed here; they are as follows: a switched-capacitor (SC) notch filter [7, 8]; an AC-coupled ripple-reduction loop (RRL) [11]; an auto-correction loop [10]; a digitally assist RRL [12]; and the combination of chopping and auto-zeroing [16, 17]. These techniques will be discussed in the following sections.

2.3.1   The Switched-capacitor (SC) Notch Filter

A simplified SC notch filter published by Burt [8] is shown in Fig. 2.8, along with its timing diagram. An SC network is placed at the output of CH_{out}. The switching frequency f_s is chosen to be the same as f_{chop}, but with a 90° phase shift (Fig. 2.8).
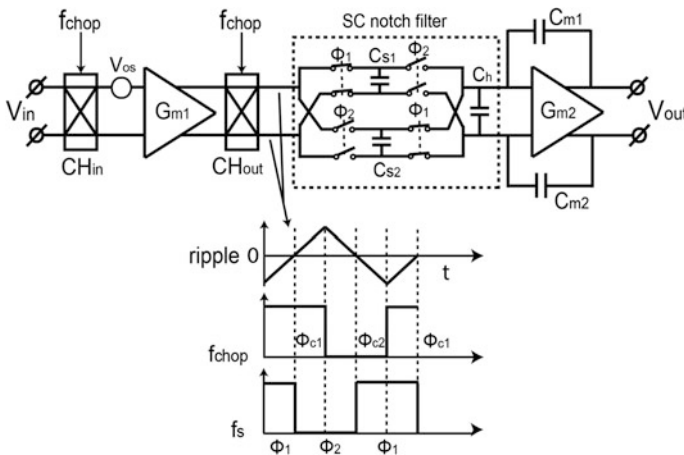

Fig. 2.8 Simplified block diagram of an amplifier employing the SC notch filter

During the first half of the chopping phase Φ_{c1}, the ripple is sampled on C_{s1}. Assuming that the ripple has a triangular shape, its amplitude will be ideally zero on the falling edge of the sampling clock f_s. At this moment, C_{s1} is disconnected from the output of CH$_{out}$ and then connected to G_{m2} until the rising edge of f_s. In this way, the ripple is not seen by G_{m2}. To obtain a quasi-continuous signal, a second sampling capacitor C_{s2}, operated in anti-phase, replicates the operation of C_{s1}. In the frequency domain, the SC network forms a narrow notch around f_{chop} in the transfer function of the amplifier. This filters out the ripple while leaving the low-frequency signal untouched. The noise introduced by the SC notch filter is mainly kT/C noise. However, since the notch filter is behind the first stage, its noise should be sufficiently suppressed by the gain of the first stage especially in the low-frequency range.

This approach is highly power efficient, since the SC network does not consume any bias current. Moreover, since it operates continuously, it is ideally immune to offset drift. However, it also has a few drawbacks. One drawback is the phase delay of the SC notch filter, which is 90° at f_{chop}. Thus, it will cause instability around f_{chop}, assuming the amplifier's bandwidth is higher than f_{chop}. As a result, a chopper stabilization architecture (Fig. 2.7) is employed by [8] and the SC notch filter is used in the LFP. In this way, the high-frequency behavior is mostly taken over by the HFP, which does not suffer from this delay. Secondly, this approach can potentially consume a large chip area. This is because a ripple voltage is integrated on $C_{s1,2}$, whose peak amplitude should be kept within the output swing of G_{m1}. For instance, with 10 mV V_{os}, 100 µS G_{m1}, and 10 kHz f_{chop}, the value of $C_{s1,2}$ required to limit the peak ripple voltage V_{ripple} within 2.5 V is:

$$C_{s1,2} = \frac{V_{off} \times G_{m1}}{2 \times f_{chop} \times V_{ripple}} = \frac{1\ \mu}{2 \times 10\ k \times 2.5} = 20\ pF \qquad (2.3)$$

The situation becomes more severe in low noise and low voltage designs, where G_{m1} must be increased and its output swing will be restricted. Increasing f_{chop} can help save chip area. However, it also results in more charge injection and clock feed-through errors, which will be explained later in Sect. 2.4.

2.3.2   *AC-Coupled Ripple-Reduction Loop*

In 2009, an AC-coupled ripple-reduction loop (RRL) was described by Wu [12]. A simplified block diagram of the RRL is shown in Fig. 2.9. It consists of two sensing capacitors $C_{s1,2}$, a demodulation chopper CH$_{RRL}$, an integrator built around G_{m3}, and a compensation transconductor G_{m4}. $C_{s1,2}$ sense the ripple and convert it into an AC current. Assuming the ripple is a triangular wave, the AC current is then a square wave as shown in Fig. 2.9. The AC current is then demodulated to DC by
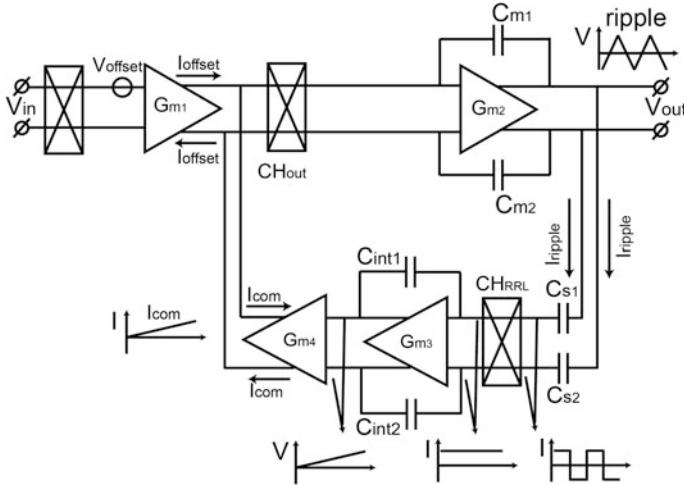
Fig. 2.9 Block diagram of the AC-coupled ripple-reduction loop

CH_{RRL} and integrated by the integrator built around G_{m3}. The output DC voltage of the integrator is then converted into a compensation current I_{com} by G_{m4}, which cancels the offset current I_{offset} of G_{m1}. When I_{com} is equal to I_{offset}, the ripple will completely disappear.

Like the SC notch filter, the RRL creates a notch at f_{chop}. The effectiveness of the RRL greatly depends on its loop gain, which in turn depends on the design parameters such as the DC gain of G_{m3}. The width of the notch can be designed by adjusting parameters such as G_{m4}, $C_{int1,2}$, and $C_{m1,2}$. A complete theoretical analysis, including the calculation of the notch width, can be found in [12].

The noise of the RRL is injected into the amplifier via G_{m4}. To minimize its contribution, G_{m4} is often designed to be much smaller than G_{m1}. However, the tail current of G_{m4} must then be sufficient to compensate for the maximum I_{offset}. Thus, G_{m4} is often biased in strong inversion or with resistor degeneration.

A problem of the circuit shown in Fig. 2.9 is the offset of the integrator built around G_{m3}. This offset will be up-modulated by CH_{RRL} and directly coupled to the output of the amplifier via $C_{s1,2}$. Thus, in reality, the circuit shown in Fig. 2.9 is hardly employed. To correct this error, the offset of G_{m3} must be removed. The methods of doing so will be introduced in Chaps. 5, 6, and 7.

The RRL is not as power efficient as the SC notch filter. However, it offers more design flexibility. The width of the notch, thus the phase delay, for instance, can be designed by adjusting several parameters such as f_{chop}, G_{m4}, $C_{int1,2}$, and $C_{m1,2}$ [12]. Moreover, it is not located in the main signal path, which makes the frequency compensation more relaxed when compared to the SC notch filter.

2.3.3 Auto-Correction Feedback Loop

This technique was first described by Kusuda [11] in 2010. A simplified block diagram is shown in Fig. 2.10. Unlike the AC-coupled RRL, the auto-correction feedback loop senses the ripple at the output of CH_{out}. In this case, a small square-wave ripple is present at the output of CH_{out}. This small ripple voltage is then sensed and converted into a current by G_{m3} and demodulated to DC by CH_{RRL}. This current is then integrated by the integrator built around G_{m4}, which is further converted into a compensating current I_{com} by G_{m5}.

However, not only the ripple but also some of the input signal will be sensed and suppressed by this loop. For instance, in the presence of a DC input signal, a DC signal voltage will appear at the input of G_{m3}, which will then be up-modulated and filtered by the integrator built around G_{m4}. A residual AC signal voltage will then be converted to an AC current by G_{m5}, which will compensate the AC signal current of G_{m1}. This can result in a significant gain reduction in the signal band. To solve this problem, a notch filter is employed which removes the up-modulated residual signal voltage at the output of G_{m4}. In this way, the DC signal is ideally not affected by the auto-correction loop.

Similar to the AC-coupled RRL, the noise of the auto-correction loop is injected into the main signal path via G_{m5}. Thus, to limit this noise, G_{m5} should be much smaller than G_{m1}.

The power efficiency of the auto-correction loop is comparable to that of the AC-coupled RRL. Sufficient ripple suppression can be guaranteed by increasing the loop gain, which in turn depends on the parameters such as the DC gain of G_{m4}.

The advantage of the auto-correction loop compared to the AC-coupled RRL shown in Fig. 2.9 is that it does not sense at the output of the amplifier. This is

Fig. 2.10 Simplified block diagram of an auto-correction loop

desired in applications where the amplifier is succeeded by a circuit that generates extra ripple at the output, such as the charge injection and clock feed-through of the input switches of a SC circuit. This extra ripple may overload the AC-coupled RRL and thus ruin its performance. The disadvantage of this approach, however, is also due to its sensing point, which is at the virtual ground instead of the amplifier's output. This means that the ripple signal is often quite small and thus a more accurate RRL with higher loop gain is required. The need for a notch filter also increases the complexity of this approach.

2.3.4 Digitally Assisted Trimming

This technique was described by Xu [13] in 2011. A simplified block diagram of this approach is shown in Fig. 2.11. After start-up, the amplifier's input is shorted, and thus, its offset voltage will be converted into an offset current I_{os} by G_{m1} and appears as a ripple at the output. The peak voltage of this ripple is sampled by a sample-and-hold (S&H) circuit and then converted into digital bits by an ADC. The digital bits are then converted into a current by a DAC, compensating I_{os}. Later, when the RRL is settled, the digital bits will be frozen and the amplifier will be connected to the signal source.

   The RRL will be shut down after it settles; thus, this approach is very power efficient. The main disadvantage of this approach is that it is vulnerable to offset drift after the RRL is frozen. Moreover, to correct the offset sufficiently, high resolution is required for both ADC and DAC, which can be tricky to implement. Reducing the resolution of the ADC/DAC will thus result in residual ripple [13].

2.3.5 Chopping + Auto-Zeroing

Before explaining the technique of combining chopping and auto-zeroing, an introduction of auto-zeroing is necessary, which will be given in the following.

Fig. 2.11 Digitally assisted RRL
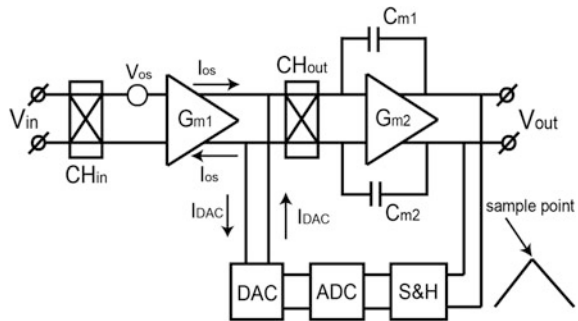
2.3.5.1   The Auto-Zeroing Principle

Auto-zeroing is also a commonly used technique to achieve low offset [1–3]. The basic principle of auto-zeroing is illustrated in Fig. 2.12. A SC network driven by a digital clock is built around an opamp G_{m1}. In the first clock phase Φ_1, G_{m1} is connected in unity-gain configuration, and its offset is thus sampled on C_{az2} and meanwhile appears at its output. In the next clock phase Φ_2, G_{m1} amplifies the input signal, and its offset V_{os} is canceled by the voltage stored on C_{az2} in Φ_1. Ideally, the voltage stored on C_{az2} should be equal to V_{os}, and thus, G_{m1} appears to be offset free. Similarly, the low-frequency $1/f$ noise components are also stored on $C_{az1,2}$ and so are canceled. However, the higher frequency $1/f$ noise components are less correlated and so cannot be effectively canceled [2].

Auto-zeroing can also be applied in an auxiliary amplifier. This is shown in Fig. 2.13 [1, 2], where an offset compensation loop is implemented around the
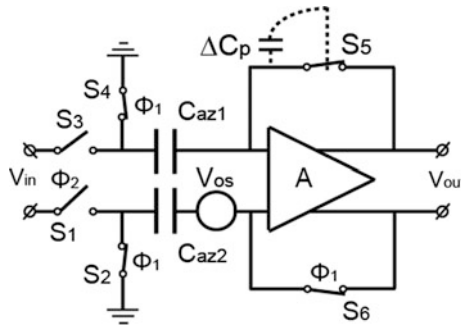

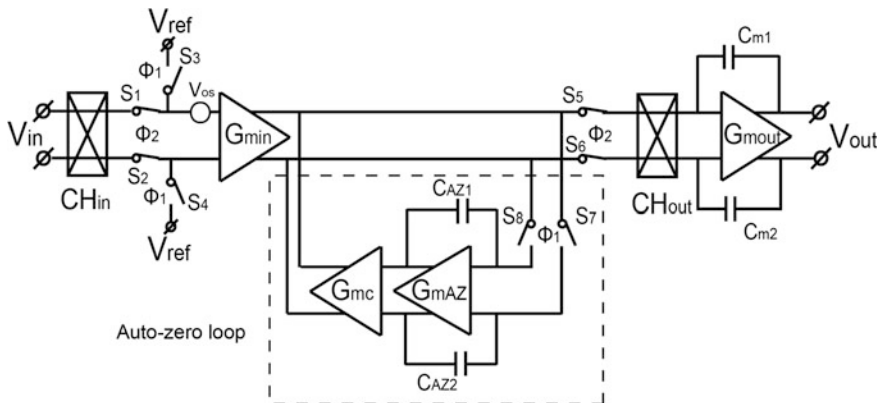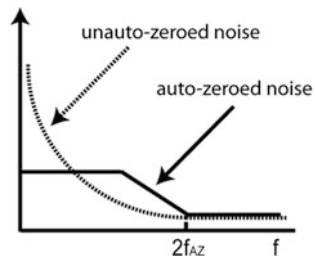Fig. 2.12   Basic block diagram of a simplified auto-zeroed amplifier

Fig. 2.13   Block diagram of an amplifier using auto-zeroing auxiliary loop

input transconductor G_{min}. In Φ_1, G_{min} is disconnected from the signal source. Its input is shorted so that its offset voltage is converted into an offset current and then integrated on the integrator built around G_{mAZ}. The output voltage of G_{mAZ} is then converted into a current by G_{mc}, which will cancel the offset current of G_{min} completely. In Φ_2, G_{min} is connected to the input signal, and the input of G_{mAZ} is disconnected from the output of G_{min}. The integrator built around G_{mAZ}, however, holds the compensation voltage stored in Φ_2, so that the offset of G_{min} is also compensated in Φ_2. The advantage of using an auto-zeroing loop rather than its simplified counterpart (Fig. 2.13) is that the errors of auto-zeroing (such as the charge injection and clock feed-through errors of $S_{5.8}$ in Fig. 2.13) are better suppressed by its high loop gain. Thus, the auto-zeroing loop is more accurate. Since there is nothing up-modulated, no ripple is expected ideally.

However, auto-zeroing has a major drawback: increased baseband noise. The sample-and-hold (S&H) action of $C_{az1,2}$ in Fig. 2.12 will result in noise folding, which increases the noise level at low frequencies [1–3]. This effect is illustrated in Fig. 2.14. It can be seen that without auto-zeroing, the low-frequency noise is dominated by the $1/f$ noise, while with auto-zeroing, the low-frequency noise is dominated by the white noise that has been folded back from high frequencies. For the complete (and rather complicated) theory of noise folding, readers are suggested to refer to [2, 18]. For amplifiers employing auto-zeroing loop shown in Fig. 2.13, however, the increased low-frequency noise can have a much smaller bandwidth by reducing the bandwidth of the auto-zeroing loop as explained in [16]. The price, however, is that the auto-zeroing loop will require a longer time to settle.

2.3.5.2 Chopping + Auto-Zeroing

From the above introduction, it is clear that auto-zeroing ideally does not introduce a ripple, but suffers from increased baseband noise. When auto-zeroing is combined with chopping, however, the increased baseband noise can be up-modulated to high frequencies. Thus, a low baseband noise floor can be obtained. This is shown in Fig. 2.15 [17] and Fig. 2.16 [16]. In [17], the increased baseband noise bandwidth is about 2× auto-zeroing frequency. Thus, the chopping frequency is chosen to be 2× auto-zeroing frequency. As a result, low noise is obtained in low frequencies. In [16], however, the auto-zeroing noise bandwidth is reduced by a slow auto-zeroing
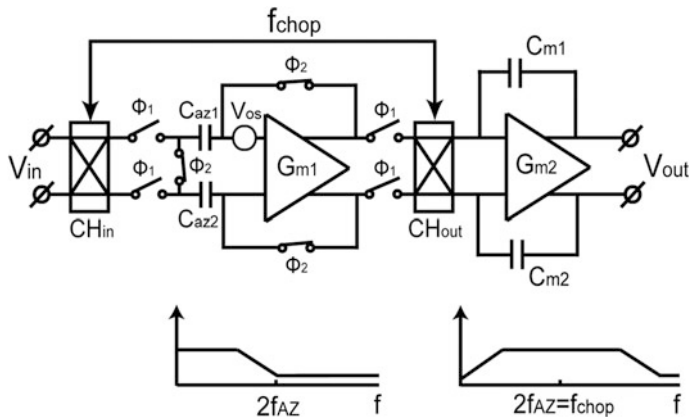
Fig. 2.15 Block diagram of a two-stage amplifier applying both chopping and auto-zeroing
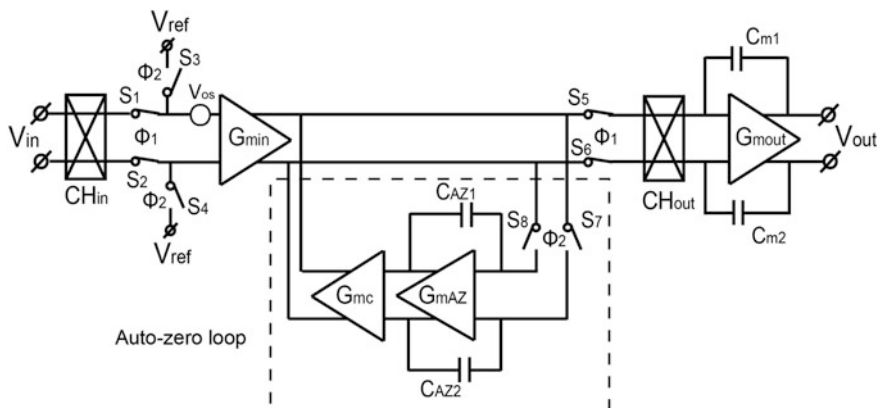

Fig. 2.16 Block diagram of an amplifier employing both chopping and auto-zero

loop. Thus, a lower chopping frequency is chosen, which results in less charge injection and clock feed-through errors.

The advantage of combing chopping and auto-zeroing is that ideally no ripple is expected and a low baseband noise can be obtained. The drawback, however, is that it does not provide continuous-time operation. To obtain continuous-time operation, a ping-pong technique should be employed [19], which involves the use of two identical input stages. During half of the auto-zeroing cycle, one input stage is being auto-zeroed, while the other is amplifying the signal. This approach, however, significantly increases the power consumption of the whole amplifier and thus is less preferred.

2.3.5.3 Summary

The presented ripple-reduction techniques all have their own advantages and disadvantages. The SC notch filter and the digitally assisted RRL are both very power efficient. However, the former suffers from a fixed phase delay and a trade-off between chopping frequency and chip area, while the latter suffers from offset drift and an accuracy compromised by the limited resolutions of the ADC/DAC. The AC-coupled RRL and the auto-correction feedback loop are less power efficient, but offer more design flexibility. Last but not least, chopping combined with auto-zeroing has a trade-off between continuous-time operation and power efficiency.

Apart from the digitally assisted RRL, the SC notch filter, the AC-coupled RRL, the auto-correction loop, and chopping combined with auto-zeroing are immune to offset drift. The basic concept shared by the SC notch filter, the AC-coupled RRL, and the auto-correction loop is the implementation of a notch filter. Thus, when they are applied in a single-path amplifier, they all create a notch in the amplifier's transfer function. And like any type of notch filter, this will result in a ringing step response (Fig. 2.17). The settling time of the ringing is determined by the relative position of the poles and zeros of the notch filter, as explained in [20]. This is undesirable in applications where fast settling is required. Thus, better techniques are required. Although chopping combined with auto-zeroing does not introduce such as notch, its power efficiency is low when continuous-time operation is required.

One solution to suppress a notch in the transfer function is to use chopper stabilization, where the HFP can be used to compensate for the loss of the gain associated with the notch. Design examples will be presented later in Chap. 5.

Fig. 2.17 Step response of a notch filter
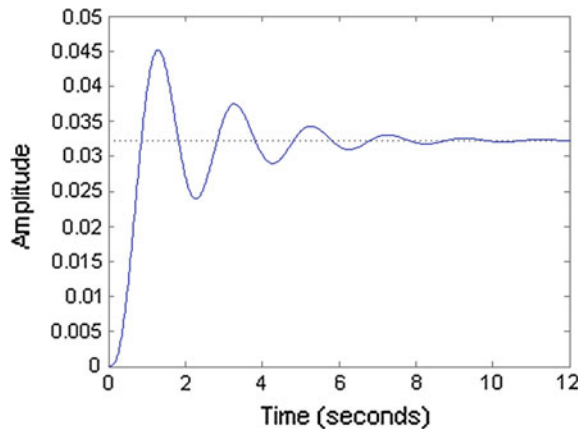
2.4 Chopping Non-idealities

Regardless of the topology employed, the chopper switches' non-idealities themselves can cause extra offset and ripple. In this section, these non-idealities will be described in detail.

First, a mismatched parasitic capacitance ΔC_{po1} (Fig. 2.18) from the clock line to one of the inputs of CH_{out} results in an AC current. This current can be modeled as an AC voltage at the input of G_{m1}, which, in turn, can be modeled as a residual offset V_{off1} at the input of CH_{in}. This can be roughly estimated as [3]:

$$V_{off1} = \frac{V_{clk} \times \Delta C_{po1} \times 2f_{chop}}{G_{m1}}. \tag{2.4}$$

For instance, with $V_{clk} = 3$ V, $\Delta C_{po1} = 1$ fF, $f_{chop} = 30$ kHz, and $G_{m1} = 100$ µS, V_{off1} is then 1.8 mV. Similarly, a mismatched parasitic capacitance ΔC_{pi1} from the clock line to one of the outputs of CH_{in} again results in an AC current, which is then demodulated by CH_{in} and converted into a voltage by the source resistance R_s. Thus, a second residual input offset V_{off2} is obtained, which can be estimated by Witte et al. [3]:

$$V_{off2} = \frac{V_{clk} \times \Delta C_{pi1} \times 2f_{chop}}{R_{on}}. \tag{2.5}$$

Furthermore, a mismatched parasitic capacitance ΔC_{po2} (Fig. 2.18) introduces an AC clock feed-through spike, which is then filtered by the integrator built around G_{m2} and appears as an output ripple. The amplitude of this ripple V_{rip1} can be estimated by:

$$V_{rip1} = \frac{V_{clk} \times \Delta C_{po2}}{C_{m1.2}}. \tag{2.6}$$

Thus, a residual ripple is obtained. Similarly, the mismatched parasitic capacitance ΔC_{pi2} again introduces an AC clock feed-through current spike at the input of the amplifier, which is then converted into a voltage by the source impedance R_s,
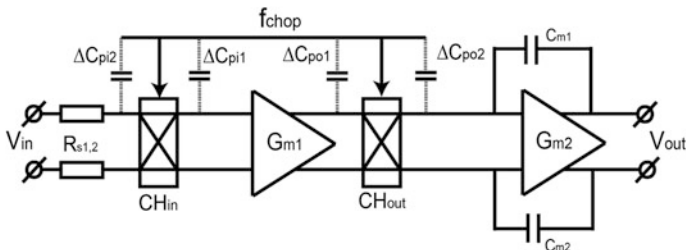

Fig. 2.18 Chopper opamp with mismatched parasitic capacitors

and then filtered by the whole amplifier and appears as another ripple V_{rip2} at the output:

$$V_{\text{rip2}} = \frac{V_{\text{clk}} \times \Delta C_{\text{pi2}} \times R_{\text{s}} \times G_{\text{m1}}}{C_{\text{m1.2}}}.$$ (2.7)

Finally, the mismatch between the chopper switches will result in mismatched charge injection errors, which have the same effects as mismatched clock feed-through as explained above. Thus, to ensure low residual errors, the layout of the choppers, including the chopper switches and the clock lines, must be as symmetrical as possible.

2.5 Chopping Pros and Cons

Chopping ensures continuous-time operation and does not necessarily introduce significant noise as explained before. However, the up-modulated offset and $1/f$ noise will produce a ripple at the output of an amplifier. Thus, ripple-reduction techniques introduced earlier should be employed. Moreover, in ultra-low noise applications, the noise of the on-resistor of the input chopper switches may not be negligible (1 kΩ ∼ 4nV/√Hz). To reduce this on-resistance, the overdrive voltage of the chopper switches or the width of the switches should be increased, which can result in more charge injection and clock feed-through errors. Last but not least, chopping can reduce the input impedance of the amplifier as shown in Fig. 2.6. In the presence of both CH_{in} and parasitic capacitors $C_{\text{p1,2}}$ at the input of G_{m1} (for instance, gate capacitance of the input pair, parasitic capacitance due to routing), a SC resistor is formed. Its DC differential resistance R_{in} can be calculated by:

$$R_{\text{in}} = \frac{1}{f_{\text{chop}} \times C_{\text{p1,2}}}.$$ (2.8)

As a result, compared to a non-chopped amplifier, a chopped amplifier's DC input impedance is lowered. To obtain a higher input impedance, lower chopping frequency and smaller $C_{\text{p1,2}}$ should be realized.

2.6 Conclusions

Based on the above, it can be concluded that by employing chopping, capacitively coupled chopper amplifiers can easily obtain low offset and low $1/f$ noise. The ripple due to chopping can also be sufficiently reduced by various ripple-reduction techniques. Building on this introduction to chopping, the working principles of capacitively coupled chopper amplifiers will be discussed in detail in Chap. 3.

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