Preface

The point where wireless communication and ubiquitous connectivity became an essential part of our lives is already past. Generation after generation communication speed is being taken to unprecedented levels, requiring both state-of-the-art hardware and software to handle a huge volume of data, delivered to an increasing number of users in an overcrowded spectrum. To our delight, the challenges are always plentiful.

With respect to the radio front-end, providing an extremely low noise emission with an improved signal integrity is a key requirement to support high-order modulation schemes (e.g., 64 QAM) in situations where anyone's transmitter can be interfering with a neighbor user or its own receiver in frequency-division full duplex mode. Increasing power and/or area consumption is not an option in this case. On the contrary, for an improved user experience the battery should last longer, and the price per component should always go down, so that more and more features can be added to a mobile/handheld device. Thus, making a better performing CMOS radio front-end that consumes even less power and area is a hot research topic these days, especially regarding the transmitter and PA designs, considered by many the "battery killers" on most mobile devices.

A quick analysis of literature shows that with regard to CMOS transmitter implementations, the state of the art is clearly divided into analog- and digital-intensive architectures. In terms of out-of-band noise, analog-intensive architectures are undoubtedly the best performing implementations. However, their improved noise performance is typically achieved through extensive low-pass filtering along the entire signal path, which has a significant impact on area consumption. Digital-intensive implementations, on the other hand, are by far the most portable, area-efficient, and scaling-friendly ones. However, the lack of filtering (for both noise and aliases) makes it very challenging to meet the stringent out-of-band noise requirements in SAW-less operation.

In this book, a novel digital-intensive transmitter architecture that can relax this trade-off is described. Through the combination of charge-domain operation with incremental signaling, this architecture gives the best of both worlds, providing the reduced area and high portability of digital-intensive architectures with an improved out-of-band noise performance given by intrinsic noise filtering capabilities.

Two implementations of the incremental charge-based TX are demonstrated, differing on how the charge-based DAC (QDAC) is implemented and the RF load being driven: In the first realization, the RF load is the input capacitance of a PPA stage, and the QDAC is implemented with a controllable capacitance that is alternately pre-charged and connected to a charge reservoir. In the second implementation, the ability of delivering more power using the charge-based architecture has been investigated with a direct-launch architecture, where the 50 Ω load representing the PA input is directly driven with charge. The QDAC is implemented with a 12-bit conductance array, which proves to be the most area-efficient implementation in this case.

Prototyped using a 28 nm 0.9 V CMOS technology, both charge-based TX realizations provide remarkable results in terms of noise performance, thanks to their intrinsic noise filtering capability, improved sampling alias attenuation, and reduced quantization noise. With an out-of-band noise spectral density of −159 dBc/Hz and a core area of 0.22 mm^2, the second implementation achieves—to the author's knowledge—the best out-of-band noise performance versus area consumption when compared to other similar works. ACLR and EVM performance are also among the best. As a result, this work paves the way for compact CMOS SAW-less transmitter implementations enabling advanced wireless communication systems, including 3G, 4G, and beyond.

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