Preface

The motivation for writing this book came as we saw that there are many books that are published related to using Xilinx software for FPGA designs. Most of these books are targeted to a specific version of Xilinx tools—be it ISE or Vivado or for a specific device. Xilinx makes two major releases of Vivado each year. Each release introduces significant new features and capabilities. Similarly, in each new device architecture, Xilinx makes significant enhancements. Hence, books written on any specific version of the software (or device architecture) get outdated very quickly. Besides, Xilinx anyways publishes its own set of documents which are updated with each major release of Vivado or FPGA architecture.

In this book, we have tried to concentrate on conceptual understanding of Vivado. These are expected to remain current through the current architecture of the tool chain. Our attempt has been that with a good conceptual understanding provided by this book, you will be able to understand the details provided in the user guides, which delve into the details of commands and options.

The Vivado software tool used for implementing a design on Xilinx's FPGAs has a lot of possible ways to read in a design. A user could describe the design in the form of HDL or "C" or make use of Xilinx-provided IP or use a third-party IP or the user could use his/her own HDL or "C" code as an IP to be used in multiple designs. A user could also describe the design using still higher level of abstractions using IP Integrator or SysGen. A design could also potentially use different types of inputs (for different portions of the design). You can use this book to understand the inherent strengths of the various modes of design entry. You can then decide which mechanism would be most suited for portions of the design. For the exact commands and syntax, you should refer to Xilinx documents. Our book provides a list of reference materials. Depending on which specific capability you plan to use, you can refer to the corresponding reference material.

Besides being useful to somebody who is new to Xilinx tools or FPGAs, the book may be found useful for those users who are migrating from ISE to Vivado. Vivado is conceptually very different from ISE. While ISE was mostly using proprietary formats for most of the flow, Vivado has moved on to industry standard formats. Users who have been long-time ISE users sometimes find it difficult to get

used to Vivado. This book helps them get a good understanding of Vivado concepts, which should make it easier for them to transition to Vivado from ISE.

Though I've been involved in some of the user guides published by Xilinx, doing this book in my personal capacity allows me to deviate from the official stand also, wherever I wanted to, and share my real opinion. ☺

The most effective way to make use of this book is to not worry about reading the book from cover to cover. You can easily feel free to skip the chapters that deal with topics which your design does not have.

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