

---

# Contents

<b>1</b>	<b>Digital Systems</b> . . . . .	1
1.1	Definition . . . . .	1
1.2	Description Methods . . . . .	4
1.2.1	Functional Description . . . . .	4
1.2.2	Structural Description . . . . .	7
1.2.3	Hierarchical Description . . . . .	8
1.3	Digital Electronic Systems . . . . .	10
1.3.1	Real System Structure . . . . .	10
1.3.2	Electronic Components . . . . .	11
1.3.3	Synthesis of Digital Electronic Systems . . . . .	18
1.4	Exercises . . . . .	18
	References . . . . .	20
<b>2</b>	<b>Combinational Circuits</b> . . . . .	21
2.1	Definitions . . . . .	21
2.2	Synthesis from a Table . . . . .	22
2.3	Boolean Algebra . . . . .	27
2.3.1	Definition . . . . .	27
2.3.2	Some Additional Properties . . . . .	30
2.3.3	Boolean Functions and Truth Tables . . . . .	31
2.3.4	Example . . . . .	34
2.4	Logic Gates . . . . .	35
2.4.1	NAND and NOR . . . . .	35
2.4.2	XOR and XNOR . . . . .	37
2.4.3	Tristate Buffers and Tristate Inverters . . . . .	41
2.5	Synthesis Tools . . . . .	42
2.5.1	Redundant Terms . . . . .	42
2.5.2	Cube Representation . . . . .	45
2.5.3	Adjacency . . . . .	47
2.5.4	Karnaugh Map . . . . .	48
2.6	Propagation Time . . . . .	50
2.7	Other Logic Blocks . . . . .	55
2.7.1	Multiplexers . . . . .	55
2.7.2	Multiplexers and Memory Blocks . . . . .	58
2.7.3	Planes . . . . .	60
2.7.4	Address Decoder and Tristate Buffers . . . . .	60

2.8	Programming Language Structures . . . . .	62
2.8.1	If Then Else . . . . .	62
2.8.2	Case . . . . .	63
2.8.3	Loops . . . . .	63
2.8.4	Procedure Calls . . . . .	65
2.8.5	Conclusion . . . . .	66
2.9	Exercises . . . . .	66
	References . . . . .	67
<b>3</b>	<b>Arithmetic Blocks . . . . .</b>	<b>69</b>
3.1	Binary Adder . . . . .	69
3.2	Binary Subtractor . . . . .	70
3.3	Binary Adder/Subtractor . . . . .	71
3.4	Binary Multiplier . . . . .	72
3.5	Binary Divider . . . . .	74
3.6	Exercises . . . . .	76
	References . . . . .	77
<b>4</b>	<b>Sequential Circuits . . . . .</b>	<b>79</b>
4.1	Introductory Example . . . . .	79
4.2	Definition . . . . .	80
4.3	Explicit Functional Description . . . . .	83
4.3.1	State Transition Graph . . . . .	83
4.3.2	Example of Explicit Description Generation . . . . .	86
4.3.3	Next State Table and Output Table . . . . .	88
4.4	Bistable Components . . . . .	88
4.4.1	1-Bit Memory . . . . .	89
4.4.2	Latches and Flip-Flops . . . . .	91
4.5	Synthesis Method . . . . .	93
4.6	Sequential Components . . . . .	96
4.6.1	Registers . . . . .	97
4.6.2	Counters . . . . .	101
4.6.3	Memories . . . . .	107
4.7	Sequential Implementation of Algorithms . . . . .	113
4.7.1	A First Example . . . . .	113
4.7.2	Combinational vs. Sequential Implementation . . . . .	116
4.8	Finite-State Machines . . . . .	119
4.8.1	Definition . . . . .	119
4.8.2	VHDL Model . . . . .	121
4.9	Examples of Finite-State Machines . . . . .	126
4.9.1	Programmable Timer . . . . .	126
4.9.2	Sequence Recognition . . . . .	129
4.10	Exercises . . . . .	132
	References . . . . .	133

---

<b>5</b>	<b>Synthesis of a Processor</b> . . . . .	135
5.1	Definition . . . . .	135
5.1.1	Specification . . . . .	135
5.1.2	Design Strategy . . . . .	136
5.2	Functional Specification . . . . .	143
5.2.1	Instruction Types . . . . .	143
5.2.2	Specification . . . . .	143
5.3	Structural Specification . . . . .	145
5.3.1	Block Diagram . . . . .	145
5.3.2	Component Specification . . . . .	147
5.4	Component Implementation . . . . .	150
5.4.1	Input Selection Component . . . . .	150
5.4.2	Computation Resources . . . . .	152
5.4.3	Output Selection . . . . .	153
5.4.4	Register Bank . . . . .	155
5.4.5	Go To Component . . . . .	158
5.5	Complete Processor . . . . .	160
5.5.1	Instruction Encoding . . . . .	160
5.5.2	Instruction Decoder . . . . .	161
5.5.3	Complete Circuit . . . . .	161
5.6	Test . . . . .	164
	References . . . . .	170
<b>6</b>	<b>Design Methods</b> . . . . .	171
6.1	Structural Description . . . . .	171
6.2	RTL Behavioral Description . . . . .	172
6.3	High-Level Synthesis Tools . . . . .	175
	References . . . . .	177
<b>7</b>	<b>Physical Implementation</b> . . . . .	179
7.1	Manufacturing Technologies . . . . .	179
7.2	Implementation Strategies . . . . .	184
7.2.1	Standard Cell Approach . . . . .	184
7.2.2	Mask Programmable Gate Arrays . . . . .	185
7.2.3	Field Programmable Gate Arrays . . . . .	185
7.3	Synthesis and Physical Implementation Tools . . . . .	188
	References . . . . .	188
	<b>Appendix A: A VHDL Overview</b> . . . . .	189
	<b>Appendix B: Pseudocode Guidelines for the Description of Algorithms</b> . . . . .	217
	<b>Appendix C: Binary Numeration System</b> . . . . .	227
	<b>Index</b> . . . . .	237



<http://www.springer.com/978-3-319-41197-2>

Digital Systems

From Logic Gates to Processors

Deschamps, J.-P.; Valderrama, E.; Terés, L.

2017, XV, 241 p. 250 illus., 33 illus. in color., Hardcover

ISBN: 978-3-319-41197-2