

Contents

1	Introduction	1
2	Switched-Capacitor Circuits	3
2.1	Switched-Capacitor Filters Building Blocks	3
2.1.1	Operational Amplifiers	3
2.1.2	Switches	3
2.1.3	Capacitors	5
2.1.4	Non-Overlapping Clock Phases	5
2.2	Switched-Capacitor Resistor Emulation Networks	5
2.2.1	Parasitic-Sensitive Integrator	7
2.2.2	Parasitic-Insensitive Integrator	8
2.2.3	Signal Flow Graph Analysis	10
2.3	Sallen-Key Topology	11
2.3.1	Low-Pass Sallen-Key Topology	12
2.3.2	Band-Pass Sallen-Key Topology	13
3	Low-Pass Filter Topologies	15
3.1	Continuous-Time Sallen-Key Low-Pass Filter	15
3.2	Switched-Capacitor Low-Pass Filter	16
3.2.1	Single-Ended Switched-Capacitor Low-Pass Filter	16
3.2.2	Differential Switched-Capacitor Low-Pass Filter	18
3.3	Switched-Capacitor Filters Using Cascaded Sections	19
3.4	Conclusions	22
4	Band-Pass Filter Topologies	23
4.1	Continuous-time Sallen-Key Band-Pass Filter	23
4.2	Switched-Capacitor Band-Pass Filter	24
4.2.1	Single-Ended Switched-Capacitor Band-Pass Filter	24
4.2.2	Differential Switched-Capacitor Band-Pass Filter	26
4.3	Switched-Capacitor Filters Using Cascaded Sections	26
4.4	Conclusions	28

5 Non-Ideal Effects	29
5.1 Non-linear Effects due to Real Switches	29
5.1.1 Filter Analysis	29
5.1.2 Simulation Results	30
5.2 Clock Boost Circuit	33
5.2.1 Clock Boost Circuit Analysis	33
5.2.2 Simulation Results	36
5.3 Low-Voltage Clock Boost Circuit	37
5.3.1 Low-Voltage Clock Boost Circuit Analysis	37
5.3.2 Simulation Results	38
5.4 Source Follower with g_{ds} Compensation	41
5.4.1 Source Follower with g_{ds} Compensation	41
5.4.2 Complementary Source Follower with g_{ds} Compensation	45
5.4.3 Source Follower with g_{ds} and Body Effect Compensation	47
5.4.4 Simulation Results	50
5.5 Low-Voltage Fully-Differential Voltage-Combiner	52
5.5.1 Fully-Differential Voltage Combiner	53
5.5.2 Complementary Fully-Differential Voltage-Combiner	57
5.5.3 Simulation Results	59
6 Switched Capacitor Filter Implementation	63
6.1 Second-Order Low-Pass SC Filter	63
6.1.1 Filter using Clock Boost and Complementary Source Follower with g_{ds} Compensation	64
6.1.2 Filter Using Low-Voltage Clock Boost and Voltage Combiner at 1.2 V	65
6.1.3 Filter Using Low-Voltage Clock Boost and Voltage Combiner at 0.9 V	67
6.2 Sixth-Order Low-Pass SC Filter	67
6.2.1 Section with Low Quality Factor	68
6.2.2 Section with Medium Quality Factor	68
6.2.3 Section with High Quality Factor	70
6.2.4 Cascaded Sections	71
6.3 Second-Order Band-Pass SC Filter	72
6.4 Fourth-Order Band-Pass SC Filter	74
6.4.1 First Filter Section	75
6.4.2 Second Filter Section	75
6.4.3 Cascaded Sections	78
7 Conclusion	79
Appendix A Butterworth Filtering Transfer Function	83
A.1 Continuous-Time Low-Pass Butterworth Transfer Function	83
A.1.1 First-Order Prototype Transfer Function	84
A.1.2 Second-Order Prototype Transfer Function	84

- A.2 Discrete-Time Low-Pass Butterworth Transfer Function 85
 - A.2.1 First-Order Prototype Transfer Function 85
 - A.2.2 Second-Order Prototype Transfer Function 86
- A.3 Continuous-Time Band-Pass Butterworth Transfer Function 86
- A.4 Discrete-Time Band-Pass Butterworth Transfer Function 87
 - A.4.1 Second-Order Prototype Transfer Function 87
- Appendix B Impulse Response Simulation and Bode Diagram Plotting** 89
- References** 91



<http://www.springer.com/978-3-319-11790-4>

Design of Switched-Capacitor Filter Circuits using Low Gain Amplifiers

Serra, H.A. de A.; Paulino, N.

2015, XIII, 92 p. 92 illus., 35 illus. in color., Softcover

ISBN: 978-3-319-11790-4