Analog filters are extremely important blocks in several electronic systems such as RF transceivers or sigma delta modulators. They allow selecting between signals with different frequency and eliminating unwanted signals.

In modern deep-submicron CMOS technologies the intrinsic gain of the transistors is low and has a large variability, making the design of moderate and high gain amplifiers extremely difficult.

The objective of this book is to study switched-capacitor (SC) circuits based on the low-pass and band-pass Sallen-Key topologies, since they do not require high gain amplifiers. The strategy used to achieve this objective is to replace the operational amplifier (opamp) with a voltage buffer. Doing this simplifies the design of the amplifier although it also eliminates the virtual ground node from the circuit. Without this node parasitic insensitive SC networks cannot be used. Due to modern parasitic extraction software that can reliably predict the values of parasitic capacitances, the historical disadvantage of parasitic sensitive SC networks (parallel SC) is no longer critical, allowing its influence to be compensated during the design process.

Different types of switches were simulated to determine the one with the least non-linear effects. Two techniques (common mode voltage adjustment and source degeneration) were used to reduce the distortion introduced by the buffers.

Low-pass (second and sixth order) and band-pass (second and fourth order) SC filters were simulated in differential configuration in standard 130 nm CMOS technology, having obtained for the low-pass filter a distortion of $-62$ dB for the biquad section and $-54$ dB for the sixth-order filter, for a cutoff frequency of 1 MHz and when operating at 100 MHz of clock frequency. The total power consumption was 986 \( \mu \text{W} \) (i.e. \( 986 \times 10^{-6} \)) and 5.838 mW, respectively.
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