Chapter 2
Switched-Capacitor Circuits

Abstract This chapter introduces SC circuits. A brief description is given for the main building blocks of a SC filter (operational amplifiers, switches, capacitors, and non-overlapping clock phases). A few examples of SC resistor emulation circuits are presented along with their equivalent resistance. Two examples of SC integrators are also shown, one with the resistors implemented with a T branch (parasitic-sensitive integrator) and another with a branch in π (parasitic-insensitive integrator). A signal flow graph is presented which allows large circuits to be analyzed graphically. The chapter ends with the two Sallen-Key topologies designed in this book, in their continuous time version.

2.1 Switched-Capacitor Filters Building Blocks

SC filters can be implemented using switches, capacitors, opamps, and non-overlapping clock generators.

2.1.1 Operational Amplifiers

Opamps in SC circuits provide a virtual ground node. Parasitic capacitances connected to this node do not influence the performance of the circuit, since they will be connected to ground during one clock phase and to the virtual ground during the other. Opamps also have non-ideal effects that affect the performance of SC circuits like DC gain, unity gain frequency and phase margin, slew-rate, and common mode voltage.

2.1.2 Switches

SC circuits require switches with high off resistance in order to minimize the charge leakage when the switches are open, and low on resistance so that the circuit can settle in less than half a clock period. MOSFET transistors satisfy both these requirements, since they have very high off resistance and low on resistance (GΩ and kΩ,

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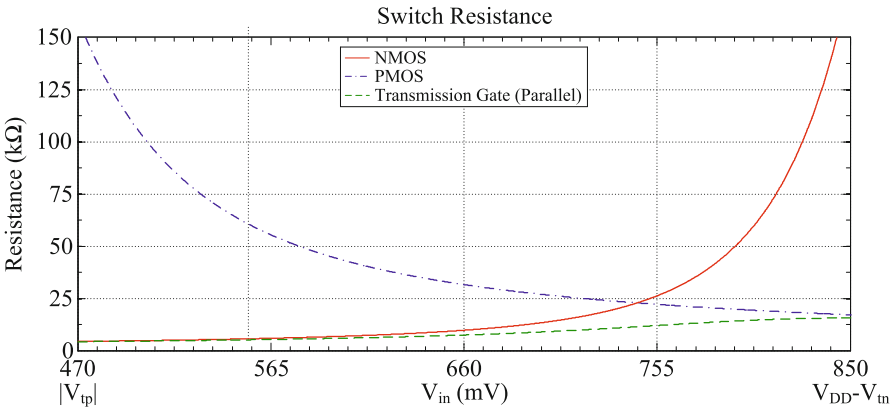


Fig. 2.1 Example of MOS transistors r_{ds} resistance as function of the $V_{in}(V_s)$ voltage

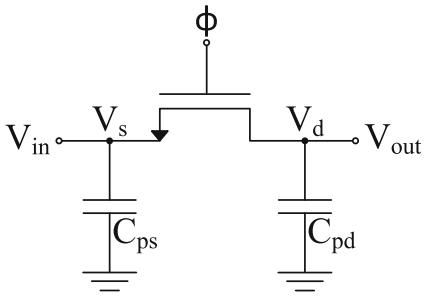


Fig. 2.2 NMOS switch model considering source and drain parasitic capacitances

respectively), depending on the transistors size. Increasing the width of the transistor will decrease the value of both of these resistances. Switches can be implemented using NMOS transistors, PMOS transistors, or both in parallel (transmission gate). Using both in parallel will decrease not only the resistance value of the switch but also improve its linearity (Fig. 2.1). While NMOS transistors are better at conducting lower voltages (logic value '0') since they stop conducting when the input voltage is close to $V_{DD} - V_{tn}$, PMOS transistors are better at conducting higher voltages (logic value '1') since they do not conduct until the voltage is higher than V_{tp}. Transmission gates are good at transmitting '0's and '1's since lower voltages will travel via the NMOS transistor and higher voltages will travel via the PMOS transistor.

Depending on the SC circuit, it may be necessary to consider the switch model including parasitics (Fig. 2.2), since they may influence the transfer function of the SC filter. Examples of SC networks that are sensitive and insensitive to these parasitic capacitances are given in Sect. 2.2. While the resistance of a switch will decrease with the increase in size of the switch, the parasitic capacitances increases. It is important to note that the parasitic capacitances of a MOS transistor are non-linear, i.e., their value varies with the applied voltage value.

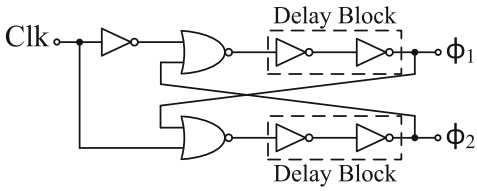


Fig. 2.3 Two-phase clock generator

2.1.3 Capacitors

Capacitors are another element for which, depending on the SC network used, it may be necessary to consider the parasitic capacitances. The bottom plate parasitic capacitance can be as high as 20 % of the capacitance value, while the top plate parasitic capacitance can be as high as 5 % [1].

2.1.4 Non-Overlapping Clock Phases

The switches present in SC circuits require at least a pair of non-overlapping clock phases to preform the charge transfer. It is required that the phases do not overlap, so that no charge is accidentally lost by having two switches closed at the same time. An example of a two-phase clock generator is shown in Fig. 2.3.

2.2 Switched-Capacitor Resistor Emulation Networks

SC circuits emulate resistors using a combination of switches and capacitors. In order to obtain the equivalent resistance it is necessary to first calculate the average current value that flows from the input into the circuit. Considering the parallel network (Table 2.1), in which the input current only flows into the circuit during half a period ($0 \leq t \leq T/2$),

$$i_{rms} = \frac{1}{T}\int_0^{T/2} i_C(t)\,\mathrm{d}t \tag{2.1}$$

Since the relation between charge and current is $\mathrm{i}(t) = \mathrm{dq}(t)/\mathrm{d}t$,

$$i_{rms} = \frac{1}{T}\int_0^{T/2} \mathrm{d}q_C(t) = \frac{Q_C(T/2) - Q_C(0)}{T} \tag{2.2}$$

Considering the phase scheme shown in Fig. 2.4, and that at $t = 0$ the capacitor maintains the voltage from the last phase, then at $t = 0 = T$ phase 2 is active and at $t = T/2$ phase 1 is active.

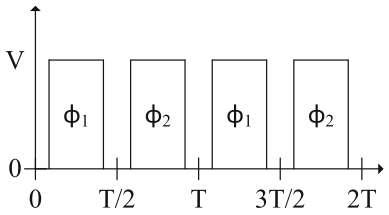


Fig. 2.4 Non-overlapping clock phase scheme

Using the charge values presented in Table 2.1 for the parallel network,

$$i_{rms} = \frac{(V_{in} - V_{out})C}{T} \tag{2.3}$$

Considering that the average current that flows through the resistance,

$$i_{rms} = \frac{V_{in} - V_{out}}{R} \tag{2.4}$$

By equating both equations (Eqs. 2.3 and 2.4) the equivalent resistance for the parallel network is obtained.

$$R_{eq} = \frac{T}{C} \tag{2.5}$$

For the networks where the current flows into the network in both phases (series-parallel and bilinear), the average current calculation must contemplate both phases. For the series-parallel network (Table 2.1),

$$\begin{aligned} i_{rms} &= \frac{1}{T}\left(\int_0^{T/2} \mathrm{d}q_{C_2}(t) + \int_{T/2}^{T} \mathrm{d}q_{C_1}(t) \right) \\ &= \frac{Q_{C_2}(T/2) - Q_{C_2}(0)}{T} + \frac{Q_{C_1}(T) - Q_{C_1}(T/2)}{T} \end{aligned} \tag{2.6}$$

Replacing the charge variables with the corresponding values that are shown in Table 2.1,

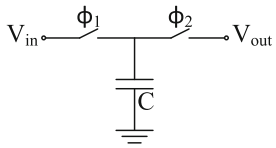
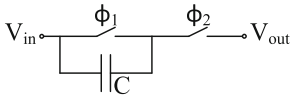
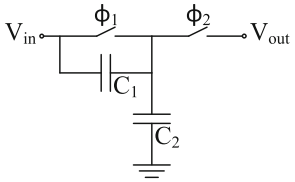
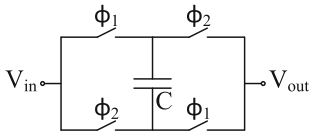
$$i_{rms} = \frac{(V_{in} - V_{out})C_2}{T} + \frac{(V_{in} - V_{out})C_1 - 0}{T} \tag{2.7}$$

and by equating Eqs. 2.7 and 2.4, the equivalent resistance for the series-parallel network is obtained.

$$R_{eq} = \frac{T}{C_1 + C_2} \tag{2.8}$$

Table 2.1 shows a few examples of circuits that can emulate resistors, their equivalent resistance, and the charge in the capacitor(s) in each phase.

Table 2.1 SC resistor emulation circuits [5]

Circuit	Schematic	R_{eq}	$Q(\varphi_1)$	$Q(\varphi_2)$
Parallel		$\frac{T}{C}$	$V_{in}C$	$V_{out}C$
Series		$\frac{T}{C}$	0	$(V_{in}-V_{out})C$
Series-Parallel		$\frac{T}{C_1+C_2}$	0 $V_{in}C_2$	$(V_{in}-V_{out})C_1$ $V_{out}C_2$
Bilinear		$\frac{1}{4}\frac{T}{C}$	$(V_{in}-V_{out})C$	$(V_{out}-V_{in})C$

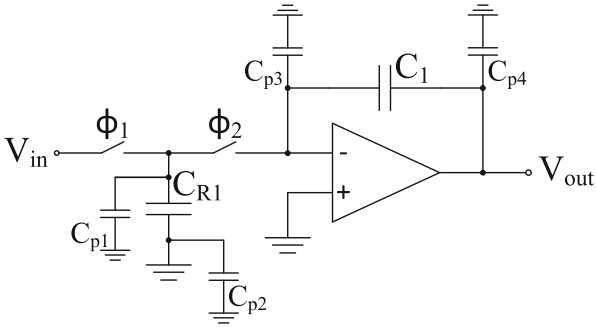


Fig. 2.5 Switched-capacitor parasitic-sensitive integrator

2.2.1 *Parasitic-Sensitive Integrator*

The SC parasitic-sensitive integrator (Fig. 2.5) was suggested in [6] by replacing the resistor in a Miller integrator with a parallel switch network.

Analyzing the charge across the capacitors in each phase, and considering that the output of the circuit will be sampled at the end of phase ϕ_1, Table 2.2 is obtained. Capacitance C_{p1} represents the top plate parasitic capacitance of C_{R1} and the parasitic

Table 2.2 Charge in the capacitors in each phase

	(n−1)T	(n−0.5)T	nT
$Q_{C_{R1}}$	$V_{in}[(n-1)T]C_{R1}$	0	$V_{in}[nT]C_{R1}$
Q_{C_1}	$-V_{out}[(n-1)T]C_1$	$-V_{out}[(n-0.5)T]C_1$	$-V_{out}[nT]C_1$
$Q_{C_{p1}}$	$V_{in}[(n-1)T]C_{p1}$	0	$V_{in}[nT]C_{p1}$
$Q_{C_{p2}}$	0	0	0
$Q_{C_{p3}}$	0	0	0
$Q_{C_{p4}}$	$V_{out}[(n-1)T]C_{p4}$	$V_{out}[(n-0.5)T]C_{p4}$	$V_{out}[nT]C_{p4}$

capacitances of both switches; capacitance C_{p2} represents the bottom plate parasitic capacitance of C_{R1}; capacitance C_{p3} represents the top plate parasitic capacitance of C_1, the input capacitance of the opamp, and the parasitic capacitance of switch ϕ_2; capacitance C_{p4} represents the bottom plate parasitic capacitance of C_1 and the input capacitance of the following stage.

Considering the transition (n−1)T → (n−0.5)T ($\phi_1 \rightarrow \phi_2$) and the transition (n−0.5)T → (n)T ($\phi_2 \rightarrow \phi_1$), Eq. 2.9 is obtained from adding all the capacitors that are connected to the virtual ground at the end of that transition (ϕ_2 in the first case and ϕ_1 in the second).

$$\begin{cases} [(n-1)T] \rightarrow [(n-0.5)T] : V_{in}[(n-1)T](C_{R1}+C_{p1}) - V_{out}[(n-1)T]C_1 = \\ \qquad = -V_{out}[(n-0.5)T]C_1 \\ \\ [(n-0.5)T] \rightarrow [nT] : -V_{out}[(n-0.5)T]C_1 = -V_{out}[nT]C_1 \end{cases} \tag{2.9}$$

Combining both equations in Eq. 2.9 and using the Z-Transform, the transfer function in Eq. 2.10 is obtained.

$$H(z) = \frac{V_{out}}{V_{in}} = -\left(\frac{C_{R1}+C_{p1}}{C_1}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right) \tag{2.10}$$

Taking into the account the parasitic capacitance, it can be seen that the gain coefficient of this circuit is dependent on C_{p1}. From the calculations it can also be concluded that the parasitic capacitance C_{p3} does not influence the performance of the circuit due to the virtual ground node in the negative node of the opamp.

2.2.2 *Parasitic-Insensitive Integrator*

To overcome the nonlinear effect of the parasitic capacitance C_{p1}, new parasitic-insensitive structures were developed [7]. Figure 2.6 shows one of these structures.

Analyzing the charge across the capacitors in each phase, and considering that the output of the circuit will again be sampled at the end of phase ϕ_1, Table 2.3

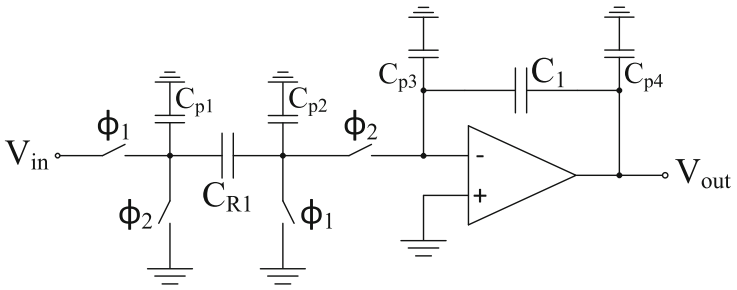


Fig. 2.6 Switched-capacitor parasitic-insensitive integrator

Table 2.3 Charge in the capacitors in each phase

	(n−1)T	(n−0.5)T	nT
$Q_{C_{R1}}$	$-V_{in}[(n-1)T]C_{R1}$	0	$-V_{in}[nT]C_{R1}$
Q_{C_1}	$-V_{out}[(n-1)T]C_1$	$-V_{out}[(n-0.5)T]C_1$	$-V_{out}[nT]C_1$
$Q_{C_{p1}}$	$V_{in}[(n-1)T]C_{p1}$	0	$V_{in}[nT]C_{p1}$
$Q_{C_{p2}}$	0	0	0
$Q_{C_{p3}}$	0	0	0
$Q_{C_{p4}}$	$V_{out}[(n-1)T]C_{p4}$	$V_{out}[(n-0.5)T]C_{p4}$	$V_{out}[nT]C_{p4}$

is obtained. Capacitance C_{p1} represents the bottom plate parasitic capacitance of C_{R1} and the parasitic capacitances of the switches connected to the bottom plate of C_{R1}; capacitance C_{p2} represents the top plate parasitic capacitance of C_{R1} and the parasitic capacitances of the switches connected to the top plate of C_{R1}; capacitance C_{p3} represents the top plate parasitic capacitance of C_1, the input capacitance of the opamp, and the parasitic capacitance of switch connected to the top plate of C_1; capacitance C_{p4} represents the bottom plate parasitic capacitance of C_1 and the input capacitance of the following stage.

Considering the transition (n−1)T → (n−0.5)T ($\phi_1 \rightarrow \phi_2$) and the transition (n−0.5)T → (n)T ($\phi_2 \rightarrow \phi_1$), Eq. 2.11 is obtained from adding all the capacitors that are connected to the virtual ground at the end of that transition (ϕ_2 in the first case and ϕ_1 in the second).

$$\begin{cases} [(n-1)T] \rightarrow [(n-0.5)T] : -V_{in}[(n-1)T]C_{R1} - V_{out}[(n-1)T]C_1 = \\ \quad = -V_{out}[(n-0.5)T]C_1 \\ \\ [(n-0.5)T] \rightarrow [nT] : -V_{out}[(n-0.5)T]C_1 = -V_{out}[nT]C_1 \end{cases} \tag{2.11}$$

Combining both equations in Eq. 2.11 and using the Z-Transform, the transfer function in Eq. 2.12 is obtained.

$$H(z) = \frac{V_{out}}{V_{in}} = \left(\frac{C_{R1}}{C_1}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right) \tag{2.12}$$

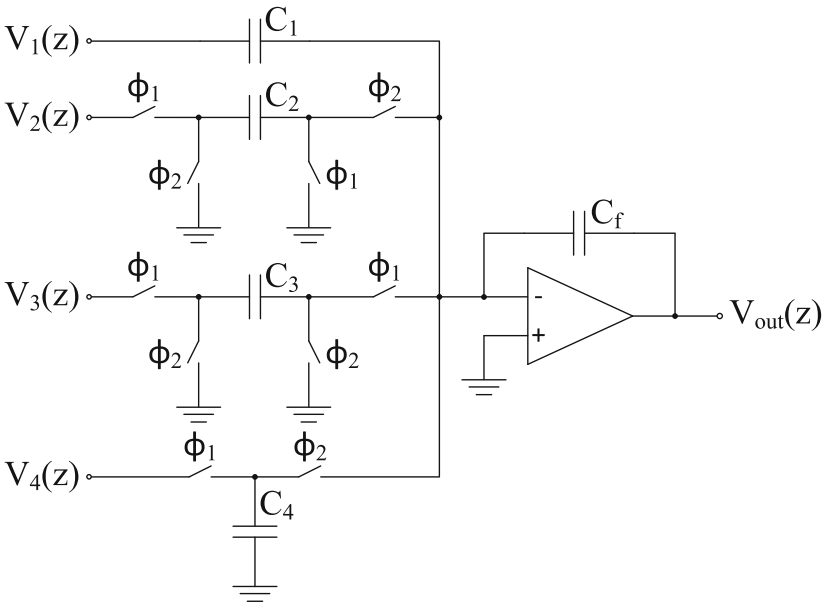


Fig. 2.7 Four-input switched-capacitor summing/integrator stage

From the calculations it can be concluded that with the addition of these two new switches the parasitic capacitances in this circuit do not influence its performance, improving the linearity of the circuit and the accuracy of the transfer function. The parasitic capacitances have little effect on the circuit since they are connected to the virtual ground (C_{p2} and C_{p3}) or the physical ground (C_{p2}). C_{p4} also has little effect since it is driven by the circuits output. Although C_{p1} is charged by the input voltage during clock phase ϕ_1, it does not affect the charge in capacitor C_{R1} since the time constant RC is long enough to charge the capacitors in less than half the clocks period, and during clock phase ϕ_2 it is discharged to ground via the ϕ_2 switch, not influencing the charge that is being transferred to C_1. Although the parasitic capacitances do not influence the circuits transfer function, they do increase the time constant RC making the settling time slower.

2.2.3 Signal Flow Graph Analysis

Using the superposition principle it is possible to determine the charge transfer functions of large circuits by analyzing the circuits graphically. Figure 2.7 shows an example of a circuit with several inputs [1].

This circuit can be analyzed using the same process as in the previous two examples. Table 2.4 shows the charge across the capacitors.

Table 2.4 Charge in the capacitors in each phase

	(n−1)T	(n−0.5)T	nT
Q_{C_f}	$-V_{out}[(n-1)T]C_f$	$-V_{out}[(n-0.5)T]C_f$	$-V_{out}[nT]C_f$
Q_{C_1}	$-V_1[(n-1)T]C_1$	$-V_1[(n-0.5)T]C_1$	$-V_1[nT]C_1$
Q_{C_2}	$-V_2[(n-1)T]C_2$	0	$-V_2[nT]C_2$
Q_{C_3}	$-V_3[(n-1)T]C_3$	0	$-V_3[nT]C_3$
Q_{C_4}	$V_4[(n-1)T]C_4$	0	$V_4[nT]C_4$

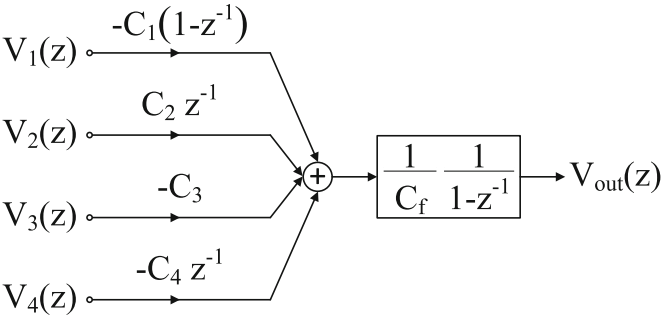


Fig. 2.8 Equivalent signal flow graph of Fig. 2.7 circuit

Analyzing the charge values in Table 2.4 individually, it is possible to obtain the charge transfer function of each subcircuit individually. These results will make it easier to analyze large circuits once the subcircuits are identified. The results of each subcircuit in Fig. 2.7 are shown in Fig. 2.8.

The signal flow graph (SFG) can be analyzed and the circuits transfer function is obtained.

$$V_{out}(z) = -\frac{C_1}{C_f}V_1(z) + \frac{C_2}{C_f}\frac{z^{-1}}{1-z^{-1}}V_2(z) - \frac{C_3}{C_f}\frac{1}{1-z^{-1}}V_3(z) - \frac{C_4}{C_f}\frac{z^{-1}}{1-z^{-1}}V_4(z) \tag{2.13}$$

2.3 Sallen-Key Topology

The SC low-pass and band-pass filters implemented in this book are based on the continuous time Sallen-Key second-order filters. In this section these topologies are presented and discussed.

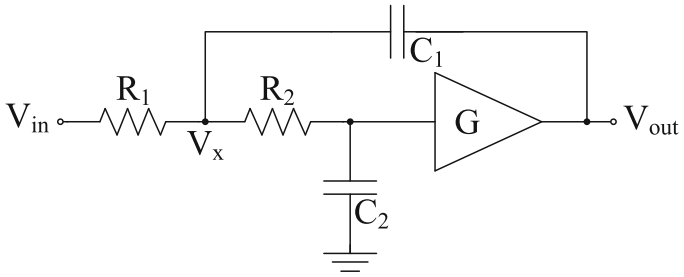


Fig. 2.9 Continuous-time Sallen-Key low-pass filter using an amplifier with gain G [8]

2.3.1 Low-Pass Sallen-Key Topology

The basis for the SC low-pass filter is the Sallen-Key low-pass filter. This filter is shown in Fig. 2.9. One of the characteristics of this type of filter is the opamp being configured as an amplifier instead of an integrator, reducing the gain-bandwidth requirements for the opamp. This means that when using this topology it is possible to implement higher frequency filters with lower gain when compared to other topologies. Another advantage of this filter is the low ratio between largest and lowest resistor/capacitor, which is important for manufacturability.

At low frequencies the capacitors can be seen as open circuits and the signal is transferred from the input to the output. At high frequency the capacitors can be seen short circuits and the signal is discharged to ground. The transfer function of this second-order filter is shown in Eq. 2.14.

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{G}{1 + (C_1R_1 + C_2R_1 - GC_1R_1 + C_2R_2)s + (C_1C_2R_1R_2)s^2} \tag{2.14}$$

Knowing that the transfer function of second order systems is

$$H(s) = G\frac{\omega_p^2}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2} \tag{2.15}$$

Using Eqs. 2.14 and 2.15, the pole frequency ω_p is

$$\omega_p = \frac{1}{\sqrt{C_1C_2R_1R_2}} \tag{2.16}$$

the inverse of the quality factor

$$\frac{1}{Q_p} = (1 - G)\sqrt{\frac{C_1R_1}{C_2R_2}} + \sqrt{\frac{C_2R_1}{C_1R_2}} + \sqrt{\frac{C_2R_2}{C_1R_1}} \tag{2.17}$$

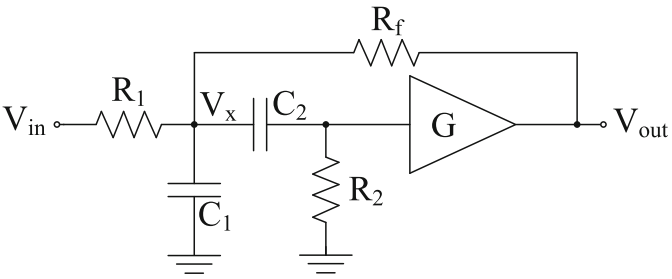


Fig. 2.10 Continuous-time Sallen-Key band-pass filter

and the low frequency gain

$$H(0) = G \tag{2.18}$$

Using these equations and selecting two of the five unknown variables it is possible to size the values of the components of the filter circuit.

2.3.2 Band-Pass Sallen-Key Topology

The basis for the SC band-pass filter is the Sallen-Key band-pass filter implemented with a voltage controlled voltage source (VCVS). The limitation of this topology is that the quality factor of the filter will determine the gain required for the amplifier. This filter is shown in Fig. 2.10.

The transfer function of this second-order filter is shown in Eq. 2.19.

$$H(s) = \frac{GC_2R_2R_fs}{R_1 + R_f + (C_1R_1R_f + C_2R_f(R_1 + R_2) - C_2R_1R_2(G-1))s + C_1C_2R_1R_2R_fs^2} \tag{2.19}$$

Where the pole frequency is

$$\omega_p = \sqrt{\frac{R_1 + R_f}{C_1C_2R_1R_2R_f}} \tag{2.20}$$

and the inverse of the quality factor

$$\frac{1}{Q_p} = \frac{C_1R_1R_f + C_2R_f(R_1 + R_2) - C_2R_1R_2(G-1)}{\sqrt{(R_1 + R_f)C_1C_2R_1R_2R_f}} \tag{2.21}$$

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