## Contents

### Part I

1. **Bias Temperature Instability Characterization Methods**  
   Andreas Kerber and Eduard Cartier  
   Page 3

2. **Application of On-Chip Device Heating for BTI Investigations**  
   Thomas Aichinger, Gregor Pobegen, and Michael Nelhiebel  
   Page 33

3. **Statistical Characterization of BTI-Induced High-k Dielectric Traps in Nanoscale Transistors**  
   Tahui Wang, Jung-Piao Chiu, and Yu-Heng Liu  
   Page 53

4. **The Time-Dependent Defect Spectroscopy**  
   Hans Reisinger  
   Page 75

5. **Analysis of Oxide Traps in Nanoscale MOSFETs using Random Telegraph Noise**  
   David J. Frank and Hiroshi Miki  
   Page 111

6. **BTI-Induced Statistical Variations**  
   Stewart E. Rauch III  
   Page 135

7. **Statistical Distribution of Defect Parameters**  
   B. Kaczer, M. Toledano-Luque, J. Franco, and P. Weckx  
   Page 161

8. **Atomic-Scale Defects Associated with the Negative Bias Temperature Instability**  
   Jason P. Campbell and Patrick M. Lenahan  
   Page 177

9. **Charge Properties of Paramagnetic Defects in Semiconductor/Oxide Structures**  
   V.V. Afanas’ev, M. Houssa, and A. Stesmans  
   Page 229

10. **Oxide Defects**  
    Jian F. Zhang  
    Page 253
11 Understanding Negative-Bias Temperature Instability from Dynamic Stress Experiments ........................................ 287
Diing Shenp Ang

Part II

12 Atomistic Modeling of Defects Implicated in the Bias Temperature Instability .................................................... 305
Al-Moatasem El-Sayed and Alexander L. Shluger

13 Statistical Study of Bias Temperature Instabilities by Means of 3D “Atomistic” Simulation ............................ 323
Salvatore Maria Amoroso, Louis Gerrer, Fikru Adamu-Lema, Stanislav Markov, and Asen Asenov

14 A Comprehensive Modeling Framework for DC and AC NBTI ...... 349
Souvik Mahapatra

15 On the Microscopic Limit of the RD Model ............................. 379
Franz Schanovsky and Tibor Grasser

16 Advanced Modeling of Oxide Defects ........................................ 409
Wolfgang Goes, Franz Schanovsky, and Tibor Grasser

17 The Capture/Emission Time Map Approach to the Bias Temperature Instability .............................................. 447
Tibor Grasser

Part III

18 Impact of Hydrogen on the Bias Temperature Instability .............. 485
Gregor Pobegen, Thomas Aichinger, and Michael Nelhiebel

19 FEOL and BEOL Process Dependence of NBTI ........................ 507
Souvik Mahapatra

20 Negative Bias Temperature Instability in Thick Gate Oxides for Power MOS Transistors .............................. 533
Ninoslav Stojadinović, Ivica Manić, Danijel Danković, Snežana Djorić-Veljković, Vojkan Davidović, Aneta Prijić, Snežana Golubović, and Zoran Prijić

21 NBTI and PBTI in HKMG .................................................. 561
Kai Zhao, Siddarth Krishnan, Barry Linder, and James H. Statthi

22 PBTI in High-k Oxides..................................................... 585
Chadwin D. Young and Gennadi Bersuker
23 Characterization of Individual Traps in High-κ Oxides .......... 597
   M. Toledano-Luque and B. Kaczer

24 NBTI in (Si)Ge Channel Devices .......................................... 615
   Jacopo Franco and Ben Kaczer

25 Characteristics of NBTI in Multi-gate FETs for Highly Scaled CMOS Technology ................................................. 643
   Ru Huang, Runsheng Wang, and Ming Li

26 Bias-Temperature Instabilities in Silicon Carbide MOS Devices ..... 661
   D.M. Fleetwood, E.X. Zhang, X. Shen, C.X. Zhang,
   R.D. Schrimpf, and S.T. Pantelides

Part IV

27 On-Chip Silicon Odometers for Circuit Aging Characterization ..... 679
   John Keane, Xiaofei Wang, Pulkit Jain, and Chris H. Kim

28 Multilevel Reliability Simulation for IC Design ......................... 719
   Ketul B. Sutaria, Jyothi B. Velamala, Venkatesa Ravi,
   Gilson Wirth, Takashi Sato, and Yu Cao

29 Charge Trapping in MOSFETS: BTI and RTN Modeling for Circuits .......................................................... 751
   Gilson Wirth, Yu Cao, Jyothi B. Velamala, Ketul B. Sutaria,
   and Takashi Sato

30 Simulation of BTI-Related Time-Dependent Variability in CMOS Circuits ......................................................... 783
   Javier Martin-Martinez, Rosana Rodriguez,
   and Montse Nafria
Bias Temperature Instability for Devices and Circuits
Grasser, T. (Ed.)
2014, XI, 810 p. 601 illus., 318 illus. in color., Hardcover
ISBN: 978-1-4614-7908-6