Contents

1 Introduction ........................................ 1
   1.1 Background ..................................... 1
   1.2 Book Motivation and Contributions .......... 3
       1.2.1 Exploration Environment for Heterogeneous
              Tree-Based FPGA Architectures .............. 5
       1.2.1 Exploration of Tree-Based ASIF Architecture .... 5
   1.3 Book Organization ................................ 6

2 FPGA Architectures: An Overview ................. 7
   2.1 Introduction to FPGAs ......................... 8
   2.2 Programming Technologies ....................... 8
       2.2.1 SRAM-Based Programming Technology ....... 9
       2.2.2 Flash Programming Technology .......... 10
       2.2.3 Anti-fuse Programming Technology .... 10
   2.3 Configurable Logic Block ....................... 11
   2.4 FPGA Routing Architectures ................. 12
       2.4.1 Island-Style Routing Architecture ...... 14
       2.4.2 Hierarchical Routing Architecture .... 19
   2.5 Software Flow ................................ 24
       2.5.1 Logic Synthesis ......................... 25
       2.5.2 Technology Mapping ....................... 26
       2.5.3 Clustering/Packing ....................... 27
       2.5.4 Placement ............................... 32
       2.5.5 Routing ................................ 36
       2.5.6 Timing Analysis ......................... 38
       2.5.7 Bitstream Generation .................... 39
   2.6 Research Trends in Reconfigurable Architectures .. 39
       2.6.1 Heterogeneous FPGA Architectures ...... 40
       2.6.2 FPGAs to Structured Architectures ...... 43
       2.6.3 Configurable ASIC Cores .................. 44
3 Homogeneous Architectures Exploration Environments

3.1 Reference FPGA Architectures
   3.1.1 Mesh-Based FPGA Architecture
   3.1.2 Tree-Based FPGA Architecture
   3.1.3 Comparison with Mesh Model

3.2 Architectures Exploration Environments

3.3 Architecture Description
   3.3.1 Architecture Description of Tree-Based Architecture
   3.3.2 Architecture Description of Mesh-Based Architecture

3.4 Software Flow
   3.4.1 Logic Optimization, Mapping and Packing
   3.4.2 Software Flow for Tree-Based Architecture
   3.4.3 Software Flow for Mesh-Based Architecture
   3.4.4 Timing Analysis
   3.4.5 Area and Delay Models

3.5 Experimentation and Analysis
   3.5.1 Architectures Optimization Approaches
   3.5.2 Effect of LUT and Arity Size on Tree-Based FPGA Architecture
   3.5.3 Comparison Between Homogeneous Mesh and Tree-Based FPGAs

3.6 FPGA Hardware Generation
   3.6.1 FPGA Generation Flow
   3.6.2 FPGA VHDL Model Generation
   3.6.3 FPGA Layout Generation

3.7 Summary and Conclusion

4 Heterogeneous Architectures Exploration Environments

4.1 Introduction and Previous Work
4.2 Reference Heterogeneous FPGA Architectures
   4.2.1 Heterogeneous Tree-Based FPGA Architecture
   4.2.2 Heterogeneous Mesh-Based FPGA Architecture

4.3 Architecture Description
   4.3.1 Architecture Description of Heterogeneous Tree-Based Architecture
   4.3.2 Architecture Description of Heterogeneous Mesh-Based Architecture

4.4 Software Flow
4.4.1 Parsers ................................................. 97
4.4.2 Software Flow for Heterogeneous
Tree-Based Architecture .......................... 100
4.4.3 Software Flow for Heterogeneous
Mesh-Based Architecture .......................... 101
4.4.4 Area Model ........................................ 103
4.5 Exploration Techniques ............................ 103
4.5.1 Exploration Techniques for Heterogeneous
Tree-Based Architecture ......................... 104
4.5.2 Exploration Techniques for Heterogeneous
Mesh-Based Architecture ......................... 106
4.6 Experimentation and Analysis .................... 108
4.6.1 Benchmark Selection ............................ 108
4.6.2 Experimental Methodology .................... 110
4.6.3 Results Using Individual Experimentation Approach ... 111
4.6.4 Results Using Generalized Experimentation Approach ... 117
4.7 Heterogeneous FPGA Hardware Generation .......... 121
4.8 Summary and Conclusion .......................... 122

5 Tree-Based Application Specific Inflexible FPGA 123
5.1 Introduction and Previous Work .................. 123
5.2 Reference FPGA Architectures .................... 125
  5.2.1 Reference Tree-Based FPGA Architecture ....... 125
  5.2.2 Reference Mesh-Based FPGA Architecture ....... 125
5.3 Software Flow ....................................... 126
5.4 ASIF Generation Techniques ...................... 126
  5.4.1 ASIF-Normal Partitioning/Placement Normal Routing . . 127
  5.4.2 ASIF-Efficient Partitioning/Placement Normal Routing . . 128
  5.4.3 ASIF-Normal Partitioning/Placement Efficient Routing . . 130
  5.4.4 ASIF-Efficient Partitioning/Placement Efficient Routing . . 132
5.5 ASIF Area Model ..................................... 132
5.6 Experimental Results and Analysis ................. 133
  5.6.1 Effect of Different ASIF Generation Techniques
  on Tree-Based Architecture ...................... 133
  5.6.2 Effect of LUT and Arity Size on Tree-Based ASIF .... 138
  5.6.3 Comparison Between Mesh-Based
  and Tree-Based ASIFs ................................ 142
  5.6.4 Quality Analysis of Tree-Based ASIF ............ 144
  5.6.5 Quality Comparison Between Mesh-Based
  and Tree-Based ASIFs .............................. 146
### 5.7 ASIF Hardware Generation
- 5.7.1 ASIF Generation Flow
- 5.7.2 ASIF VHDL Model Generation
- 5.7.3 ASIF Layout Generation
- 5.8 Summary and Conclusion

### 6 Tree-Based ASIF Using Heterogeneous Blocks
- 6.1 Reference Heterogeneous FPGA Architectures
  - 6.1.1 Heterogeneous Tree-Based FPGA Architecture
  - 6.1.2 Heterogeneous Mesh-Based FPGA Architecture
  - 6.1.3 Software Flow
- 6.2 Heterogeneous ASIF Generation Techniques
- 6.3 Experimentation and Analysis
  - 6.3.1 Experimental Benchmarks
  - 6.3.2 Effect of Different ASIF Generation Techniques on Heterogeneous Tree-Based ASIF
  - 6.3.3 Effect of LUT and Arity Size on Heterogeneous Tree-Based ASIF
  - 6.3.4 Comparison Between Heterogeneous Mesh-Based and Tree-Based ASIFs
- 6.4 Quality Analysis of Heterogeneous Tree-Based ASIF
  - 6.4.1 Quality Comparison Between Heterogeneous Mesh-Based and Tree-Based ASIF
- 6.5 Heterogeneous ASIF Hardware Generation
- 6.6 Summary and Conclusion

### 7 Conclusion and Future Lines of Research
- 7.1 Summary of Contributions
  - 7.1.1 Heterogeneous Tree-Based FPGA Exploration Environment
  - 7.1.2 Tree-Based ASIF Exploration
  - 7.1.3 FPGA and ASIF Hardware Generation for Tree-Based Architecture
- 7.2 Suggestions for Future Research
  - 7.2.1 Datapath Oriented FPGA Architectures
  - 7.2.2 Timing Analysis
  - 7.2.3 Integrating ASIF Blocks in an FPGA Architecture
  - 7.2.4 Further Optimizing the ASIF Generation
  - 7.2.5 The Unexplored Parameters of Mesh-Based Architecture
- References
Tree-based Heterogeneous FPGA Architectures
Application Specific Exploration and Optimization
Farooq, U.; Marrakchi, Z.; Mehrez, H.
2012, XVI, 188 p., Hardcover
ISBN: 978-1-4614-3593-8