Contents

1 Introduction ........................................ 1
   1.1 Background ...................................... 1
   1.2 Book Motivation and Contributions ............... 3
      1.2.1 Exploration Environment for Heterogeneous
            Tree-Based FPGA Architectures ............... 5
      1.2.1 Exploration of Tree-Based ASIF Architecture .. 5
   1.3 Book Organization .................................. 6

2 FPGA Architectures: An Overview ..................... 7
   2.1 Introduction to FPGAs ............................ 8
   2.2 Programming Technologies ......................... 8
      2.2.1 SRAM-Based Programming Technology ......... 9
      2.2.2 Flash Programming Technology ............... 10
      2.2.3 Anti-fuse Programming Technology .......... 10
   2.3 Configurable Logic Block ......................... 11
   2.4 FPGA Routing Architectures ....................... 12
      2.4.1 Island-Style Routing Architecture .......... 14
      2.4.2 Hierarchical Routing Architecture .......... 19
   2.5 Software Flow ..................................... 24
      2.5.1 Logic Synthesis ................................ 25
      2.5.2 Technology Mapping ........................... 26
      2.5.3 Clustering/Packing ............................ 27
      2.5.4 Placement ...................................... 32
      2.5.5 Routing ........................................ 36
      2.5.6 Timing Analysis ................................ 38
      2.5.7 Bitstream Generation ......................... 39
   2.6 Research Trends in Reconfigurable Architectures .. 39
      2.6.1 Heterogeneous FPGA Architectures ........... 40
      2.6.2 FPGAs to Structured Architectures .......... 43
      2.6.3 Configurable ASIC Cores ....................... 44
4.4.1 Parsers ............................................. 97
4.4.2 Software Flow for Heterogeneous
    Tree-Based Architecture ......................... 100
4.4.3 Software Flow for Heterogeneous
    Mesh-Based Architecture .......................... 101
4.4.4 Area Model ....................................... 103
4.5 Exploration Techniques ............................. 103
    4.5.1 Exploration Techniques for Heterogeneous
          Tree-Based Architecture ...................... 104
    4.5.2 Exploration Techniques for Heterogeneous
          Mesh-Based Architecture ...................... 106
4.6 Experimentation and Analysis ...................... 108
    4.6.1 Benchmark Selection .......................... 108
    4.6.2 Experimental Methodology .................... 110
    4.6.3 Results Using Individual Experimentation Approach ... 111
    4.6.4 Results Using Generalized Experimentation Approach ... 117
4.7 Heterogeneous FPGA Hardware Generation ............ 121
4.8 Summary and Conclusion ............................ 122

5 Tree-Based Application Specific Inflexible FPGA .......... 123
    5.1 Introduction and Previous Work .................. 123
    5.2 Reference FPGA Architectures .................... 125
        5.2.1 Reference Tree-Based FPGA Architecture ...... 125
        5.2.2 Reference Mesh-Based FPGA Architecture ...... 125
    5.3 Software Flow .................................... 126
    5.4 ASIF Generation Techniques ....................... 126
        5.4.1 ASIF-Normal Partitioning/Placement Normal Routing ... 127
        5.4.2 ASIF-Efficient Partitioning/Placement
              Normal Routing .................................. 128
        5.4.3 ASIF-Normal Partitioning/Placement
              Efficient Routing .................................. 130
        5.4.4 ASIF-Efficient Partitioning/Placement
              Efficient Routing .................................. 132
    5.5 ASIF Area Model ................................... 132
    5.6 Experimental Results and Analysis .................. 133
        5.6.1 Effect of Different ASIF Generation Techniques
              on Tree-Based Architecture ...................... 133
        5.6.2 Effect of LUT and Arity Size on Tree-Based ASIF ...... 138
        5.6.3 Comparison Between Mesh-Based
              and Tree-Based ASIFs ............................ 142
        5.6.4 Quality Analysis of Tree-Based ASIF .............. 144
        5.6.5 Quality Comparison Between Mesh-Based
              and Tree-Based ASIFs ......................... 146
6 Tree-Based ASIF Using Heterogeneous Blocks .................. 153
6.1 Reference Heterogeneous FPGA Architectures .......... 153
  6.1.1 Heterogeneous Tree-Based FPGA Architecture .... 154
  6.1.2 Heterogeneous Mesh-Based FPGA Architecture .... 154
  6.1.3 Software Flow .................................. 155
6.2 Heterogeneous ASIF Generation Techniques ............. 155
6.3 Experimentation and Analysis .......................... 156
  6.3.1 Experimental Benchmarks .......................... 156
  6.3.2 Effect of Different ASIF Generation Techniques on Heterogeneous Tree-Based ASIF .......... 157
  6.3.3 Effect of LUT and Arity Size on Heterogeneous Tree-Based ASIF ............................ 161
  6.3.4 Comparison Between Heterogeneous Mesh-Based and Tree-Based ASIFs .................. 164
6.4 Quality Analysis of Heterogeneous Tree-Based ASIF ...... 166
  6.4.1 Quality Comparison Between Heterogeneous Mesh-Based and Tree-Based ASIF ............ 168
6.5 Heterogeneous ASIF Hardware Generation .................. 168
6.6 Summary and Conclusion .............................. 171

7 Conclusion and Future Lines of Research ................... 173
7.1 Summary of Contributions .............................. 173
  7.1.1 Heterogeneous Tree-Based FPGA Exploration Environment ......................... 174
  7.1.2 Tree-Based ASIF Exploration ....................... 174
  7.1.3 FPGA and ASIF Hardware Generation for Tree-Based Architecture .................. 176
7.2 Suggestions for Future Research ......................... 177
  7.2.1 Datapath Oriented FPGA Architectures ............... 177
  7.2.2 Timing Analysis .................................. 178
  7.2.3 Integrating ASIF Blocks in an FPGA Architecture .... 179
  7.2.4 Further Optimizing the ASIF Generation ............ 179
  7.2.5 The Unexplored Parameters of Mesh-Based Architecture ......................... 180

References .................................................. 181
Tree-based Heterogeneous FPGA Architectures
Application Specific Exploration and Optimization
Farooq, U.; Marrakchi, Z.; Mehrez, H.
2012, XVI, 188 p., Hardcover
ISBN: 978-1-4614-3593-8