Preface

High-speed analog-to-digital converters have become essential components of all communication systems. While we typically think of information as sequences of discrete digital symbols, the behavior of the transmission channels in all modern systems does not conform to this abstraction. Especially when a data link is pushed toward its limits, the received signals are a complex mix of wanted and unwanted analog waveforms that must be disentangled by ever more complex equalization (and channel selection) schemes. In wireless and long-distance wireline communications, these receive-side signal processing tasks have long been dealt with in the digital domain. Only recently, however, digital-domain equalization has also gained momentum in short-distance wired links providing up to several tens of gigabit/second connectivity between computer servers and their constituent components. When going digital, the designer of these links can reap the benefits of improved programmability and increased filter lengths. On the other hand, the burden is now placed on the analog-to-digital converter, which must now be inserted to finely digitize the incoming analog waveforms in order to make them fit for digital interpretation.

This monograph captures the state-of-the-art knowledge on how such high-performance converters can be realized in modern CMOS technology. Specifically, it describes how the core concepts of time-interleaving and mismatch calibration can be leveraged to achieve energy efficient conversion at sample rates of 10 GSample/second and beyond. In the discussed implementation of a 5-bit, 12-GSample/second analog-to-digital converter, several modern and innovative enhancement techniques are employed. The first is a novel statistics-based timing calibration technique that aligns the sampler timing in the ADC's input path to within a fraction of 1 ps (the time it takes for light to travel about 0.3 mm!). The second is a device-offset calibration scheme that leverages the integration density of nanometer CMOS by employing about 250 auxiliary D/A converters for component trimming. In combination, these techniques have yielded one of the most efficient data converters for high-speed links published to date.

Composed with a well-balanced mix of theoretical analysis and practical design guidelines, this book will be a valuable resource for any circuit designer active in the development of high-speed interfaces.

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