# Contents

1 Challenges of Power Electronic Packaging ........................................ 1
   1.1 Challenges of Power Semiconductor Packaging ....................... 2
       1.1.1 Impact of Power Die Shrinkage ................................ 3
       1.1.2 Power System on Chip vs. System in Package ............... 3
       1.1.3 Power Package Foot Print Pitch vs. PCB Pad Pitch ......... 4
       1.1.4 New Materials for Power Device .............................. 5
       1.1.5 New Materials for Power Package .............................. 6
   1.2 Summary ........................................................................ 7
   References ........................................................................... 7

2 Power Package Electrical Isolation Design .................................... 9
   2.1 Background ..................................................................... 9
   2.2 Design Rule for Isolation .................................................. 11
       2.2.1 Protection with Insulation ....................................... 11
       2.2.2 Solid and Air Insulation ......................................... 12
       2.2.3 Design Rule of Clearance and Creepage ..................... 13
   2.3 Estimation of the Clearance and Creepage Distances .............. 17
       2.3.1 Required Major Functions ...................................... 17
       2.3.2 Determine the Clearance and Creepage ....................... 19
   2.4 Packaging Design Layout Consideration .............................. 21
   2.5 Safety Standards and Categories of Application .................... 23
   2.6 Summary ..................................................................... 25
   References ........................................................................... 25

3 Discrete Power MOSFET Package Design and Analysis ................... 27
   3.1 An Example of a TO Power Package: Design, Assembly,  
       and Mount Process ........................................................... 27
   3.2 The Trend of Using Epoxy Mold Compound ............................ 32
   3.3 Trends of Current Carrying Capability, Low $R_{ds(on)}$,  
       and Multiple Direction Heat Transfer ................................ 35
3.4 Typical Discrete Power Package Designs and Constructions ........ 39
  3.4.1 The SO-8 Wireless Power Package ................................ 39
  3.4.2 The Flip Chip Leaded Molded Package ....................... 40
  3.4.3 The MOSFET BGA ................................................. 43
3.5 Power VDMOSFET WL-CSP with Cu Stud Bumping .............. 44
  3.5.1 The Cu Stud Bumping Construction on a Power WL-CSP ...... 44
  3.5.2 Investigation of BPSG Design Profile Under the Al Layer and FAB Size on Cu Stud Bumping Process ....................... 45
3.6 The Trends of Discrete Power VDMOSFET WL-CSP .......... 54
  3.6.1 Ultrathin Silicon Substrate and Thick Back Metal .......... 54
  3.6.2 Move the MOSFET Drain to Front Side .................... 54
3.7 Summary .................................................................. 55
References ....................................................................... 56

4 Power IC Package Design and Analysis .............................. 57
  4.1 The Evolution of the Power IC Technology ..................... 57
  4.2 Higher Power Density at the Die Level ....................... 61
  4.3 Smaller Package Footprints ...................................... 67
  4.4 Typical Package Design and Analysis for Power IC .......... 71
    4.4.1 MLP Design and Construction ............................... 71
    4.4.2 Design and Thermal Analysis of Premolded MicroPak MLP ........ 74
    4.4.3 Package Substrate Design for Reliability ............... 77
    4.4.4 Challenges in Wire Bonding Process for Package with Laminate Substrate ........................................ 78
    4.4.5 Wafre Level Chip Scale Package for Power IC .......... 82
  4.5 Summary .................................................................. 88
References ....................................................................... 88

5 Power Module/SiP/3D/Stack/Embedded Packaging Design and Considerations ........................................ 89
  5.1 Side by Side Placement Power System in Package/Module ...... 89
    5.1.1 Lower Power Driver MOSFET System in Package ...... 89
    5.1.2 Hybrid Power System in Package Module ............... 104
  5.2 Power Stack Die System in Package .............................. 123
    5.2.1 The Design Concept of the Power Stack Die SiP ........ 124
    5.2.2 TMCL Solder Joint Reliability Analysis ................... 127
    5.2.3 Failure Analysis of the Power Module .................... 134
    5.2.4 Discussion ............................................................ 136
  5.3 Wafer Level Power Stack Die 3D Package with TSV .......... 136
    5.3.1 The Design Concept of the Wafer Level Power Stack Die Package ........................................ 137
    5.3.2 Thermal Analysis ...................................................... 138
    5.3.3 Stress Analysis in Assembly Process ...................... 140
5.4 Stack and Embedded Die Power Module ........................................ 152
  5.4.1 The Design Concept of the Stack and Embedded Die Power Package ........................................ 153
  5.4.2 Thermal Performance Evaluation .................................... 155
  5.4.3 The Stress Assessment After the Molding Process ............... 156
  5.4.4 The Preconditioning Stress Analysis ............................. 160
5.5 Summary ........................................................................... 165
References ............................................................................. 165

6 Thermal Management, Design, and Cooling for Power Electronics ................................. 167
  6.1 Thermal Resistance and Measurement Methods .................. 167
    6.1.1 Thermal Resistance Concept .................................. 167
    6.1.2 Temperature Sensitive Parameter (TSP) Method for Junction Calibration .................................. 169
    6.1.3 Thermal Resistance Measurement Procedure ............... 171
    6.1.4 Thermal Resistance Measurement Environments ............ 173
  6.2 Selection of a Thermal Test Board .................................... 175
    6.2.1 Low-Effective Thermal Test Board ............................ 176
    6.2.2 High-Effective Thermal Test Board ............................ 176
    6.2.3 Thermal Test Board for Various Power Packages .......... 177
    6.2.4 Standards for Thermal Test Board .............................. 178
  6.3 Thermal Prediction, Management and Design ...................... 182
    6.3.1 Estimation of Junction Temperature .......................... 182
    6.3.2 Estimation of the Maximum Power Dissipation .......... 183
    6.3.3 Thermal Management and Design for Power Package ....... 183
  6.4 Heat Transfer Analysis from Device to Board Level ............ 191
    6.4.1 SOI Device Operation and Design Consideration .......... 191
    6.4.2 FEA Modeling Analysis for the SOI Device and SO Assembly Package Level .............................. 193
    6.4.3 Thermal Modeling Results and Discussion ................... 194
    6.4.4 Equivalent Resistance Method with Thermal Net .......... 199
  6.5 Multiple-Die Thermal Analysis ......................................... 202
    6.5.1 Multiple-Die Thermal Resistance Definition ............... 202
    6.5.2 Application of a Power Multiple-Die Thermal Resistance ........................................ 203
  6.6 Cooling for Power Packaging ............................................ 206
    6.6.1 Air Flow Cooling .............................................. 206
    6.6.2 Other Cooling Methods ....................................... 211
  6.7 Summary ........................................................................... 212
References ............................................................................. 213
7 Material Characterization for Power Electronics Packaging

7.1 Effect of Polyimide Coating on a MOSFET Die

7.1.1 Issues of the Polyimide and EMC Materials

7.1.2 Assumptions, Material Properties, and Analysis Method

7.1.3 Analysis Model Without Considering the Silica Fillers in Mold Compound Material

7.1.4 Simulations Considering Silica Fillers in Mold Compound Material

7.2 Die Attach Stress Analysis and Material Selection

7.3 Epoxy Mold Compound Characterization

7.3.1 Behavior of Epoxy Mold Compound Material

7.3.2 Experimentation of Epoxy Mold Compound

7.3.3 Test Result, Modeling, and Discussion

7.4 Mechanical and Thermal Behavior of Ceramic/DBC Substrate

7.4.1 Ceramic Substrate in a Power Package

7.4.2 DBC Substrate

7.4.3 Thermal Performance of Ceramic vs. DBC

7.5 Solder Material Characterization

7.5.1 Introduction of the Solder Material Characterization

7.5.2 Solder Material Viscoplastic Constitutive Relation: Anand Model

7.5.3 Experiment Procedure

7.5.4 The Test and Characterization Results

7.5.5 Anand Model Parameter Data Fitting

7.5.6 Modified Anand Model Parameter

7.5.7 Discussions and Other Solder Materials

7.6 Lead Frame Material Characterization

7.7 Summary

References

8 Power Package Typical Assembly Process

8.1 Wafer Handling Process

8.2 Die Pickup

8.3 Die Attach

8.3.1 Material Constitutive Relations

8.3.2 Die Attach Model and Reflow Profile

8.3.3 FEA Simulation Result of Flip Chip Attach

8.4 Wire Bonding

8.4.1 Assumption, Material Properties, and Method of Analysis

8.4.2 Ball Wire Bonding Process with Different Parameters

8.4.3 Optimization of Wedge Bonding for a Power Package
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.5</td>
<td>Molding</td>
<td>323</td>
</tr>
<tr>
<td>8.5.1</td>
<td>Molding Flow Simulation and Analysis</td>
<td>323</td>
</tr>
<tr>
<td>8.5.2</td>
<td>Molding Ejection</td>
<td>330</td>
</tr>
<tr>
<td>8.6</td>
<td>Power Package Trim/Singulation</td>
<td>332</td>
</tr>
<tr>
<td>8.6.1</td>
<td>Punch Process Setup</td>
<td>333</td>
</tr>
<tr>
<td>8.6.2</td>
<td>Punch Process Analysis by LS-DYNA</td>
<td>335</td>
</tr>
<tr>
<td>8.6.3</td>
<td>Experimental Data</td>
<td>338</td>
</tr>
<tr>
<td>8.7</td>
<td>Summary</td>
<td>342</td>
</tr>
<tr>
<td>References</td>
<td>343</td>
<td></td>
</tr>
</tbody>
</table>

9 Power Packaging Typical Reliability and Test

9.1 Power Packaging Reliability and Test in General

9.1.1 Reliability Life                                         | 345  |
9.1.2 Failure Rate                                            | 346  |
9.1.3 Typical Reliability Tests for Power Package             | 348  |

9.2 Power and Thermal Cycling

9.2.1 Background                                             | 357  |
9.2.2 Die Attach Process and Material Relations               | 358  |
9.2.3 Power Cycling Modeling and Discussion                  | 360  |
9.2.4 Thermal Cycling Modeling and Discussion                | 364  |

9.3 Power Packaging Passivation Crack Analysis

9.3.1 Ratcheting Deformation Mechanism                        | 374  |
9.3.2 Growth of the Crack and Critical Width                  | 383  |
9.3.3 Design Modification                                    | 384  |
9.3.4 Discussion                                             | 386  |

9.4 Power Packaging Wafer Probing Test and Analysis

9.4.1 2D Analysis Model                                       | 387  |
9.4.2 Simulation Results and Discussion of 2D Model           | 389  |
9.4.3 3D Model                                                | 391  |
9.4.4 Simulation Results and Discussion of 3D Model           | 393  |

9.5 Influence of Heat Sink Mounting Procedure on Power Package Reliability

9.5.1 Background                                             | 396  |
9.5.2 A Model of Heat Sink Mounting                          | 396  |
| for Power Packaging                                       | 397  |
9.5.3 Impact of Lead Frame Design to Package Reliability     | 399  |
9.5.4 Impact of Lead Frame Material Property                | 401  |
9.5.5 Actual Heat Sink Mounting Test                        | 405  |
9.5.6 Discussion                                             | 405  |

9.6 ACLV Moisture Analysis of Power Package

9.6.1 Solder Overflow in Die Attach Process and Finite Element Models Description | 406  |
9.6.2 Effect of Solder Overflow                               | 409  |
9.6.3 Effect of Mold Compound                                | 413  |
9.6.4 Process Improvement and Experimental Data              | 413  |
9.7 Drop Test Reliability of Wafer Level Chip Scale Package
9.7.1 WL-CSP Drop Test and Analysis Model Setup
9.7.2 Drop Impact Simulation/Test with Different Design Variable and Discussion
9.7.3 Drop Test
9.8 Summary

References

10 Power Packaging Modeling and Challenges
10.1 Modeling Role in Power Electronic Industry
10.2 Challenges of Modeling Tools and Methodology
10.2.1 Challenges of Modeling Tools
10.2.2 Numerical Methods of Tools
10.2.3 The Next Step of Modeling Tool
10.3 Modeling Requirements in Semiconductor
10.3.1 Front-End Process Modeling
10.3.2 Power Device Modeling
10.3.3 Modeling of Interconnects Passives
10.3.4 Circuits Modeling
10.3.5 Power Package Level Simulation
10.4 Modeling Methodologies Needed in Power Packaging
10.4.1 The Methodologies of Power Packaging
10.4.2 The Methodologies of Power Packaging
10.5 Advanced Modeling Techniques
10.5.1 Finite Element Method
10.5.2 Advanced Modeling Techniques in Finite Element Analysis
10.5.3 Finite Element Application in Semiconductor Packaging Modeling
10.6 Modeling Trends in Power Electronic Packaging
10.6.1 Codesign Automation Simulation
10.6.2 Advanced Modeling Methodologies in Power Packaging
10.6.3 Multiphysics and Multiscale Modeling
10.7 Summary

References

11 Power Package Thermal and Mechanical Codesign Simulation Automation
11.1 Power Package Thermal Modeling and Test Correlation
11.1.1 Background
11.1.2 Thermal Resistance Test Procedure

References
11.1.3 Influence of Each Factor in Thermal Resistance Test ........................................ 468
11.1.4 Package Solid Model .................................................. 469
11.1.5 Material Properties and Boundary Conditions .......... 469
11.1.6 Discussion of the Thermal Simulation and Correlation ...................................... 475

11.2 Wafer Level Power Package Parameter Thermal Simulation ................................................ 475
11.2.1 Background for the Power WL-CSP Thermal Analysis ...................................................... 476
11.2.2 Construction of the Parametric Model .................................................. 477
11.2.3 Thermal Automation by Using ANSYS APDL .................................................. 480
11.2.4 Application of the Parametric Model .................................................. 482
11.2.5 Thermal Simulation Analysis .................................................. 483
11.2.6 Result Discussion .................................................. 490

11.3 Package Thermal, Mechanical, Hygroscopic, and Vapor Pressure Codesign Automation Simulation ........... 491
11.3.1 Background of the Codesign Automation .......................... 491
11.3.2 Basic Formulations .......................................................... 493
11.3.3 Development of Automated Codesign Simulation System for Thermal, Mechanical, Moisture, and Vapor Analysis .................................................. 496
11.3.4 Application of AutoSim .................................................. 503

11.4 Summary ................................................................. 514
References.................................................................................. 515

12 Power Package Electrical and Multiple Physics Simulation ........... 517
12.1 Power Package Electrical Simulation .................................................. 517
12.1.1 Extracting the Inductance and Resistance ...................... 518
12.1.2 Methodology for Extracting Capacitance ...................... 525

12.2 Defect Impact on Power Package Electrical Performance ........... 532
12.2.1 Background .......................................................... 532
12.2.2 Resistance, Inductance and the Fusing Current .......... 533
12.2.3 Impact of Wire Bonding Related Defect ...................... 534
12.2.4 Impact of Die Attach Solder Void ...................... 541
12.2.5 Discussion and Conclusions .................................................. 543

12.3 Power UIL/UIS Test and Simulation .................................................. 545
12.3.1 Background .......................................................... 545
12.3.2 DC Test .......................................................... 546
12.3.3 AC Test .......................................................... 549
12.3.4 Fusing Current Test.................................................. 549
12.3.5 UIL Test .......................................................... 551
12.3.6 Discussion and Conclusion .................................................. 555
Power Electronic Packaging
Design, Assembly Process, Reliability and Modeling
Liu, Y.
2012, XVIII, 594 p., Hardcover