# Preface

The Internet communication service is being extended beyond its traditional frontiers of fixed wired infrastructure through the gradual addition of a broad range of complex networks and autonomous devices. In particular, the introduction of the Smartphone and subsequently the Tablets has produced a demand for mobile data services that has been growing rapidly. From traditional wireless networks to opportunistic networks of mobile devices in dense environments, new hardware platform requirements are becoming increasingly more complex, due to the necessary processing and computation power. The need for revolutionary or evolutionary architectures with multiple processors designed using different types of processors and technologies, and thus managing a range of heterogeneous components in order to support new multimedia services are only a subset of the wide range of existing new technologies that require high levels of processing power.

The consequence of the evolution of the mobile wireless standards is an increased need for the system to support multiple standards and multi-component devices for backward compatibility. These two requirements greatly complicate the development of telecommunication systems, imposing the optimization of device parameters over numerous constraints, such as performance, area and power. Achieving device optimization requires a deep understanding of application complexity and the choice of an appropriate architecture to support this application.

Of particular note, the new, feature-rich wireless standard called long-term evolution (LTE) is a complex application that needs a large amount of processing power. LTE is the next evolutionary step after 3G for mobile wireless communication, and is aimed at increasing the wireless network capacity while improving the spectral efficiency. LTE unites many technological innovations from diverse research areas such as digital signal processing, Internet protocols, network architecture, and security, and, as such, will drastically change the way that the worldwide mobile network is used in the future. LTE is anticipated to be the first truly global wireless standard, as it may be deployed in a variety of spectrum and operating scenarios, and has the capability to support a myriad of wireless applications. Numerous operators and service providers around the world have already deployed LTE on their networks or have announced LTE as their intended next generation technology.

An LTE eNodeB or base station must use powerful embedded hardware platforms, to offer a complete feature set with reasonable cost and power. Multi-core digital signal processors (DSP) combine cores with processing flexibility and hardware coprocessors that accelerate complex functionalities or repetitive processes, and, as such, are suitable hardware architectures to execute complex operations in real-time. The focus of this study is the physical layer portion of LTE eNodeB, so to understand the dynamism and the parallelism of this application under specific constraints such as latency.

The novel method of rapid prototyping was designed to alleviate the long simulation times now required in device optimization for complex architectures. It consists of studying the design tradeoffs at several stages of the development, including the early stages, when the majority of the hardware and software is not available. Initially, the inputs to a rapid prototyping process must be models of system parts, and are much simpler than in the final implementation. In a perfect design process, programmers would enlarge the models progressively, heading towards the final implementation.

Imperative languages, particularly C, are presently the preferred languages to program DSPs. Decades of compilation optimizations have refined these languages resulting in a good tradeoff between readability, optimality and modularity. However, imperative languages have been developed to address sequential hardware architectures inspired by the Turing machine and their ability to express algorithm parallelism is limited. Alternatively, dataflow languages and models have proven over many years to be efficient representations of parallel algorithms, thus allowing the simplification of their analysis.

This work proposes a novel top-down approach to tackle the multicore programming issue; it uses the rapid prototyping method and dataflow language for the simulation and code generation processes. Building on the base generated by other authors, the rapid prototyping method, which permits study of LTE signal processing algorithms, is constructed and explained. The relevant signal processing features of the physical layer of the 3GPP LTE telecommunication standard are then detailed. The next important building block in this novel approach is the dataflow model of computation, which is the model used to describe the application algorithms in this study. This new methodology is then contrasted with the existing techniques for system programming and rapid prototyping.

The System-Level Architecture Model (S-LAM) is a topology graph which defines data exchanges between the cores of a heterogeneous architecture. This S-LAM architecture model is developed to feed the rapid prototyping method. Additionally, a scheduler structure is detailed; this structure allows the separation of the different aspects of multi-core scheduling, in addition to providing other improvements to state-of-the-art methods. The scheduler developed in this study has the capacity to schedule the dynamic algorithms of LTE at run-time. The subsequent analysis using the methodology based on these blocks is two-fold:

firstly the LTE rapid prototyping and simulation, and then the code generation. The code generation is divided into two parts; the first deals with static code generation, and the second with the adaptive scheduler driven by a multi-core operating system.

The role of this work is to contribute a new methodology to a problem that will be ever more present. Software rapid prototyping methods were developed to replace certain tedious and suboptimal steps of the current test-and-refine methodologies for embedded software development. In this study, these new techniques were successfully applied to 3GPP LTE eNodeB physical layers. As such, this work has an important place in the study of optimal deployment of dynamic parallel applications, particularly those targeting LTE eNodeB lower layers, onto multi-core-based device architectures.

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http://www.springer.com/978-1-4471-4209-6

Physical Layer Multi-Core Prototyping
A Dataflow-Based Approach for LTE eNodeB
Pelcat, M.; Aridhi, S.; Piat, J.; Nezan, J.-F.
2013, XVI, 212 p., Hardcover
ISBN: 978-1-4471-4209-6