Preface

3D integration technologies, 3D-Design techniques, and 3D-Architectures are emerging as truly hot and broad research topics. As the end of scaling the CMOS transistor comes in sight, the third dimension may come to the rescue of the industry to allow for a continuing exponential growth of integration during the 2015–2025 period. As such 3D stacking may be the key technology to sustain growth until more exotic technologies such as nanowires, quantum dot devices and molecular computers become sufficiently mature for deployment in main stream application areas.

The present book gathers the recent advances in the domain written by renowned experts to build a comprehensive and consistent book around the topics of three-dimensional architectures and design techniques.

In order to take full advantage of the 3D integration, the decision on the use of in-circuit vertical connection (predominantly Through-Silicon-Vias (TSVs) and Inductive Wireless Interconnects) must come upfront in the architecture planning process rather than as a packaging decision after circuit design is completed. This requires taking the 3D design space into account right from the start of the system design. Previously published books about this active research domain focus on fabrication technologies and physical aspects, rather than network and system-level architectural concerns. In contrast, the present book covers almost all architectural design aspects of 3D-SoCs, and as such can be useful both for introducing the current research topics to researchers and engineers, giving a basis for education and training in M.Sc. and Ph.D. programs.

The book is divided into three parts. The first part, which contains two chapters, deals with the promises and challenges of 3D integration. Chapter 1 introduces 3D integration of Integrated Circuits, and as an objective, discusses performance enhancement, as well as new integration capabilities, enabled technology platforms, and potential applications made possible by 3D technology. Chapter 2 elaborates on the promises and limitation of 3D integration by studying the limits of performance under different memory distribution constraints of various 2D and 3D topologies in current and future technology nodes.

The second part of the book consists of four chapters. It discusses technology and circuit design of 3D integration. Chapter 3 focuses on the available solutions and open challenges for testing 3D Stacked ICs (3D-SICs). It provides an overview
of the manufacturing steps of TSV-based 3D-SICs relevant for the testing issues. Chapter 4 reviews the process of 3D-IC designing exploiting Through-Silicon-Via technology, and introduces the notion of re-architecting systems explicitly to exploit high density TSV processes. Chapter 5 investigates physical properties of NoC topologies for 3D integrated systems. It describes an enhanced physical analysis methodology, providing a means to estimate early in the design cycle the behavior of a 3D topology for an integrated system interconnected with an on-chip network. Chapter 6 characterizes the performance of multiple 3D NoC architectures in the presence of realistic traffic patterns through cycle-accurate simulation and establishes the performance benchmark and related design trade-offs.

The last part of the book includes five chapters that globally concern system and architecture design of 3D integration. Chapter 7 makes a case for using asynchronous circuits to implement 3D-NoCs. It claims that asynchronous logic allows for serializing vertical links, leading to the definition of innovative architectures which, by reducing the number of TSVs, can address some critical issues of 3D integration. Chapter 8, by supporting both unicast and multicast traffic flows, considers the problem of designing application-specific 3D-NoC architectures that are optimized for a given application. Chapter 9 presents methodologies and tools for automated 3D interconnect design, focusing on application-specific 3D-NoC synthesis which consists of finding the best NoC topology for the application, computing paths for the communication flows, assigning network components onto the layers of the 3D stack, and placing them in each layer. Chapter 10 describes constructing 3D-NoCs based on inductive-coupled wireless interconnect in which the data modulated by a driver are transferred between two inductors placed at exactly the same position of two stacked dies. Chapter 11 discusses how 3D technology can be implemented in GPUs. It investigates the problems and constraints of implementing such a technology and proposes architectural designs for a GPU that implements 3D technology and evaluates these designs in terms of fabrication cost, power consumption and thermal profile.

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