Designing an application-specific multi-core System-on-Chip is a tricky endeavor and requires to make dozens of system level decisions with profound impact on performance and cost at an early time in the design phase, when many details are still unknown and performance estimates are notoriously inaccurate. Technology development is progressing and is continuously increasing our raw computing capacity. At the same time application requirements and standards become more demanding. Together this leads to complex designs that require sophisticated and continuously developed architectures, tools, and methodologies.

In particular since the field during the last decade has embarked to massively increase the number of heterogeneous cores, the picture has become very complicated. Moreover, it is quickly changing with respect to demands on architectures and tools. Hence, the design technology seems to fall more and more behind manufacturing technology, which is also referred to as the design productivity gap and illustrated in Fig. 1a. In order to get to grips with this disturbing situation, researchers have tried to develop scalable architectures and tools that continue to be efficient and usable even as the number of cores dramatically grows. The promise of scalable architectures or tools is that we can use them in 2011 with 20 or 50 cores, and we can still use them in 2017 with 200 or 500 cores. Once a scalable architecture for an application domain or a scalable tool for a design problem has been developed, the design research stops running behind the semiconductor manufacturing advances and can truly focus on exploiting the given capabilities of technology, as illustrated in Fig. 1b.

The European FP7 MOSART project (http://www.mosart-project.org/) has set as its goal to develop scalable solutions to architectures, tools, and methodologies. Figure 2 gives an overview of the MOSART design flow and also indicates which parts are covered in this book. Even though not all the work of the project are fully documented here, several important results of our work on architecture and hardware (Part I), system level design and exploration (Part II), and applications (Part III) are reported.
The MOSART project was a joint effort from January 2008 till December 2010 by partners from industry (Thales Communication in Paris, Intracom in Athens, Arteris in Paris, and CoWare/Synopsys in Belgium and Germany), Research institutes (IMEC in Leuven and VTT in Oulu), and Universities (ICCS in Athens and KTH in Stockholm). Based on the combined competence, the team had the ambition to push new techniques in multi-core architecture platforms and design tools. Inspired from the applications provided by Thales and Intracom, as described in Chaps. 7 and 8, several innovations have been developed and demonstrated. A major part of these innovations are summarized in this book, and we sincerely hope it will be useful and stimulating for researchers and industrial practitioners in the area.

We would like to extend our gratitude to all members of the MOSART team for an exciting project collaboration, many inspiring discussions, and for the warm company at many meetings between mild Rhodes Island in the South and chilly Oulu in the North of Europe. We want to thank the authors for the contributions and the hard work on the chapters of this book making it into a concise and representative summary of 3 years of research and development. Furthermore, we would like to express our appreciation for the project reviewer’s comments and feedback that were always insightful and to the point, and that greatly helped us to stay focused, to increase our efforts, and to keep our overall objectives in mind. They have certainly contributed to make the results of higher quality. We would also like to thank our project officers (Ms. Zulema Olivan-Tomas and Ms. Margot Bezz) for their professional and sensible handling of MOSART, and last but not least, we are very grateful to the team of Springer who has enthusiastically supported this book from the very beginning, very professionally transformed the material into a high quality publication, and kept patience and support when the delivery of the material were behind schedule.
Fig. 2  Multi-core SoC design flow

Most importantly we hope that you, the reader, will enjoy reading this book and it triggers inspiration and many new ideas.

Athens and Stockholm

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