Transmission line (TL) effects are one of the most common causes of noise problems in high-speed DSP systems. When do traces become TLs and how do TLs affect the system performance? A rule-of-thumb is that traces become TLs when the signals on those traces have a rise-time (Tr) less than twice the propagation delay (Tp). For example, if a delay from the source to the load is 2nS, then any of the signals with a rise-time less than 4nS becomes a TL. In this case, termination is required to guarantee minimum overshoots and undershoots caused by reflections. Excessive TL reflections can cause electromagnetic interference and random logic or DSP false-triggering. As a result of these effects, the design may fail to get the FCC certification or to fully function under all operating conditions such as at high temperatures or over-voltage conditions.

There are two types of transmission lines, lossless and lossy. The ideal lossless transmission line has zero resistance while a lossy TL has some small series resistance that distorts and attenuates the propagating signals. In practice, all TLs are lossy. Modeling of lossy TLs is a difficult challenge that is beyond the scope of this book. Since the focus of this book is only on practical problem-solving methods, it assumes a lossless TL to keep things simple. This is a reasonable assumption because in DSP systems where the operating frequency is less than 1GHz the losses on printed circuit board traces are negligible compared to losses in the entire signal chain, from analog to digital and back to analog.
2.1 TRANSMISSION LINE THEORY

A lossless TL is formed by a signal propagating on a trace that consists of series parasitic inductors and parallel capacitors as shown in Figure 2.1.

![Lossless Transmission Line Model](image)

Figure 2.1. Lossless Transmission Line Model

The speed of the signal, $V_p$, is dependant on properties such as characteristic impedance, $Z_o$, which is defined as an initial voltage $V^+$ divided by the initial current $I^+$ at some instant of time. The Eqs. (2.1) and (2.2) for $V_p$ and $Z_o$ are

$$V_p = \frac{1}{\sqrt{LC}}, \quad (2.1)$$

$$Z_o = \sqrt{\frac{L}{C}}, \quad (2.2)$$

where $L$ is inductance per unit length and $C$ is capacitance.

Another important property of the TL is the propagation delay, $T_d$. The Eq. (2.3) for $T_d$ is

$$T_d = \frac{1}{V_p} = \sqrt{LC}. \quad (2.3)$$

The source and load TL reflections depend on how well the output impedance and the load impedance, respectively, are matched with the characteristic impedance. The load and source reflection coefficients, Eq. (2.4) and Eq. (2.5), are
\[ \Gamma_S = \text{source}\_\text{reflections} = \frac{Z_S - Z_O}{Z_S + Z_O}, \quad (2.4) \]

\[ \Gamma_L = \text{load}\_\text{reflections} = \frac{Z_L - Z_O}{Z_L + Z_O}, \quad (2.5) \]

where \( Z_S \) and \( Z_L \) are the source impedance and load impedance respectively.

The following example shows the characteristics of a TL with no load and with a 3V signal source driving the line.

**Example 2.1:** Calculate the voltage at the open ended load of the transmission line below.

\[
\begin{align*}
V_{\text{cl}} &= V_{\text{clk}} \cdot \frac{Z_O}{Z_S + Z_O} = 3 \cdot \frac{50}{25 + 50} = 2V \\
\rho_S &= \frac{Z_S - Z_O}{Z_S + Z_O} = \frac{25 - 50}{25 + 50} = -0.333 \\
\rho_L &= \frac{Z_L - Z_O}{Z_L + Z_O} = 1
\end{align*}
\]

**Figure 2.2.** Open Ended Transmission Line
In Figure 2.3, the overshoot voltage can be calculated using a lattice diagram [1] as follows.

At $T_1 = 1.8nS$: $V_L = V_i + \rho_L V_i = 2 + 2 = 4.0V$,

At $T_2 = 3.6nS$: $V_S = 4.0V + \rho_S V_i = 4.0V - 0.67V = 3.33V$,

At $T_3 = 5.4nS$: $V_L = 3.33V + \rho_L(\rho_S V_i) = 3.33 - 0.67 = 2.66V$,

At $T_4 = 7.2nS$: $V_S = 2.66V + \rho_S[\rho_L(\rho_S V_i)] = 2.66 + 0.22 = 2.88V$,

At $T_5 = 9.0nS$: $V_L = 2.88 + \rho_L (0.22) = 3.1V$

![Lattice Diagram of Open Ended TL](image-url)
As shown in Example 2.1, the reflections with a 3V source caused the signal to overshoot as high as 4V at the load as explained below:

- The initial voltage level at the load at time T1 depends on the load impedance, which is infinite for an open load, and the characteristic impedance of the TL.
- The voltage level at time T2, when the reflected signal arrives at the source, depends on the source impedance and the characteristic impedance of the TL.
- The voltage level at time T3, when the reflected signal arrives at the load again, depends on the reflected voltage at T2 plus the reflected voltage at time T3.
- This process continues until steady state is reached. In this example, the steady state occurs at T5, which is 9nS from T1, as shown in Figure 2.3.
Figure 2.5 shows the waveforms at the load for both terminated and unterminated circuits. As shown in the previous example, the terminated TL has a zero reflection coefficient and therefore no ringing occurs on the waveform as seen on the top graph of Figure 2.5. The problem is that in high-speed digital design, adding a 50-ohm resistor to ground at the load is not practical because this requires the buffer to drive too much current per line. In this case, the current would be \( \frac{3.3V}{50} = 66mA \). A technique known as parallel termination can be used to overcome this problem. It consists of adding a small capacitor in series with the resistor at the load to block DC. The RC combination should be much less than the rise and fall times of the signal propagating on the trace.

![Figure 2.5. Voltage Waveforms at the Terminated and Unterminated Loads](image)

![Figure 2.6. Parallel Termination with Multiple Loads](image)
Figure 2.6 shows a parallel termination technique. This method can be used in the application where one output drives multiple loads as long as the traces to the loads called L2 are a lot shorter than the main trace L1.

To use the parallel termination technique, it is necessary to calculate the maximum allowable value for L2 according Eq. (2.6) below assuming the main trace L1 and the rise-time Tr are known.

$$L_2, \text{max} = L_1^{10^{\frac{t_r}{10}}}$$  \hspace{1cm} (2.6)

### 2.2 PARALLEL TERMINATION SIMULATIONS

Parallel termination techniques become useful when designers have to use a single clock output to drive multiple loads to minimize the clock skew between the loads. In this case, having a series resistor at the source limits the drive current to the loads and may cause timing violations by increasing rise-times and fall-times. This simulation example includes one 6” trace (L1) and two 2” stubs. The DSP [2] drives the main L1 trace and one memory device connected to each end of the 2” trace. It is reasonable to neglect the effects of the stubs as long as they are short and meet the criteria shown in Figure 2.7. In this case, only one parallel termination (68 ohms and 10pF) is required at the split of the main trace to the loads. Referring to the simulation result in Figure 2.8, the waveforms at the loads look good and meet all the timing requirements for the memory devices. As expected for the “no series” termination case, the waveform at the source does not look good but this does not affect the system integrity at the load.

---

**Figure 2.7. Parallel Termination Configuration**
Figure 2.8. Parallel Termination Simulation Results

Figure 2.9 shows an example of one clock output driving two loads connected using a daisy-chain topology. The distance from the source to the first load (1st SDRAM) is the same as the distance from the first load to the second load (2nd SDRAM). In this case, the reflections coming from the second load distort the clock signal at the first load. The best way to minimize this distortion is by adding a parallel termination at the second load to reduce the impedance mismatch and therefore reduce the reflections as shown in Figures 2.10 and 2.11. This system still requires a series termination at the source to control the edge rate of the whole signal trace. This resistor needs to be small so that the source and sink currents are large enough to drive two loads. In this example, the series termination resistor is 10 ohms.

Figure 2.9. DSP Clock Driving Two Loads
2.3 PRACTICAL CONSIDERATIONS OF TL

In general, high-speed DSP systems consist of many CMOS devices where the input impedance is very high, typically in Mega ohms and the input capacitance is relatively small, less than 20pF. In this case, with no load termination, the TL looks like a transmission line with a capacitive load, rather than an open circuit. The capacitive load helps reduce the rise-time and allows the designers to use only a series termination at the source. This approach is becoming very common in high-speed systems.
In Figure 2.12, the voltage at the load is slowly charged up to the maximum amplitude of the clock signal. Initially, the load looks like a short circuit. Once the capacitor is fully charged, the load becomes an open circuit. The source resistor $Z_s$ controls the rise and fall-times. Higher source resistance yields slower rise-time. The load voltage at any instant of time, $t$, greater than the propagation delay time, can be calculated using the following equation:

$$V_L = V_{clk} \left(1 - e^{-\frac{(t-T_d)}{\tau}}\right),$$  \hspace{1cm} (2.7) $$

where $t$ is some instant of time greater than the propagation delay and $\tau = C_l Z_o$, where $C_l$ and $Z_o$ are the load capacitor and characteristic impedance respectively.

2.4 SIMULATIONS AND EXPERIMENTAL RESULTS OF TL

2.4.1 TL Without Load or Source Termination

One of the well-known techniques to analyze the PC board is using a signal integrity software [3] to simulate the lines. Figure 2.13 shows a setup used for the simulations.
The selected signal is FLASH.CLK which is a clock signal generated by a DSP. Figure 2.14 shows an actual PC board designed with a DSP where the clock is driven by U3 and is measured at U2.

Figure 2.14. PC Board Showing FLASH.CLK Trace

Figure 2.15 shows the simulation result at U2 and Figure 2.16 shows the actual scope measurement in the lab.
2.4.2 TL with Series Source Termination

As discussed earlier, most high-speed system designs use this technique. Since, it is possible to optimize the load waveforms simply by adjusting the series termination resistors. This technique also helps reduce the dynamic power dissipation, since the initial drive current is limited to the maximum source voltage divided by the characteristic impedance. Figure 2.17 shows the setup used for the simulation of the audio clock driven by an audio CODEC external to the DSP.
Figure 2.17. Series Termination Clock Setup

Figure 2.18 shows an audio clock that transmits by U17 and receives by U3. The design has a 20-ohm series termination resistor but no parallel termination at the load. This demonstrates the concept discussed earlier.

Figure 2.18. Audio Clock with Series Termination

The simulation result is shown in Figure 2.19.
Figure 2.19. Series Termination Simulation Result

The lab measurement shown in Figure 2.20 correlates with the simulation very well. The 22-ohm series resistor can be modified to lower the overshoots and undershoots. But since the overshoots are less than 0.5V, they are acceptable in this case.

Figure 2.20. Series Termination Lab Measurement
2.5 GROUND GRID EFFECTS ON TL

In summary, the simulation results correlate very well with the actual lab measurements. Designers need to understand the TL characteristics and terminate traces to minimize reflections that may cause random circuit failures, excessive noise injected into the power, ground planes and electromagnetic radiation.

One final comment about the TL is that the previous examples were based on a model where a signal trace is on top of a ground plane known as a microstrip model. Other techniques, such as a ground grid, are also commonly used. Example 2.2 demonstrates the effects of the ground grid. In this configuration, the designers need to understand the current flows and their effect on the characteristic impedance.

Example 2.2:

Figure 2.21 shows an example of using a ground grid, instead of ground plane for the PC board. As shown in this figure, the current path is not immediately under the signal trace, so there is a large current return loop that yields higher inductance and lower capacitance per unit length. In this case, the characteristic impedance is higher than if a continuous ground plane was used.

![Current Return Paths of Ground Grid](image)

Figure 2.21. Current Return Paths of Ground Grid
Figure 2.22 also shows another example of using a ground grid where the signal is being routed diagonally. As shown in this figure, the current return has to travel on a zig zag pattern back to the source and creates a large current return loop that yields higher inductance and lower capacitance per unit length. In this case, the characteristic impedance is higher than using a continuous ground plane and higher than the case where the signal is routed in parallel with the ground grid as shown in Figure 2.21.

![Current Return Paths of Diagonal Grid](image)

**Figure 2.22. Current Return Paths of Diagonal Grid**

So, if ground grid is a required in a design, the best approach is to route the high speed signals right on top of the grids and parallel to the grid to ensure the smallest current return loops. This lowers the characteristic impedance to the level equivalent to the impedance of the continuous ground plane. This is very difficult to accomplish since complex board has many high speed traces. Therefore, continuous ground plane is still the best method to keep characteristic impedance and EMI low.

### 2.6 MINIMIZING TL EFFECTS

As demonstrated in this chapter, transmission line effects cause signal distortions which may lead to digital logic failures and radiations. These effects can’t be eliminated totally but can be minimized by applying the following guidelines:

- Slow down the signal edge rate by lowering the buffer drive strength if it is not affecting the timing margins. Remember a
trace becomes a TL if the rise-time of the signal propagating on it is less than a roundtrip propagation delay.

- If the edge rate of the buffer is not configurable, add a series termination resistor as close to the source as possible. The value of the resistor is equal to the characteristics impedance ($Z_o$) of the trace minus the buffer output impedance.

- When one clock is driving multiple loads as shown in Figure 2.9, add a series termination at the source and a parallel termination at the load.

- If ground grids have to be used, route the high speed signals in parallel with the ground grids to reduce the current return loops. Ground planes are always preferred over ground grids.
REFERENCES


High-Speed DSP and Analog System Design
Tran, T.T.
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