This monograph is motivated by the challenges faced in designing reliable VLSI systems in modern VLSI processes. The reliable operation of integrated circuits (ICs) has become increasingly difficult to achieve in the deep submicron (DSM) era. With continuously decreasing device feature sizes, combined with lower supply voltages and higher operating frequencies, the noise immunity of VLSI circuits is decreasing alarmingly. Thus, VLSI circuits are becoming more vulnerable to noise effects such as crosstalk, power supply variations, and radiation-induced soft errors. Among these noise sources, soft errors (or error caused by radiation particle strikes) have become an increasingly troublesome issue for memory arrays as well as combinational logic circuits. Also, in the DSM era, process variations are increasing at a significant rate, making it more difficult to design reliable VLSI circuits. Hence, it is important to efficiently design robust VLSI circuits that are resilient to radiation particle strikes and process variations. The work presented in this research monograph presents several analysis and design techniques with the goal of realizing VLSI circuits, which are radiation and process variation tolerant.

This monograph consists of two parts. The first part proposes four analysis and two design approaches to address radiation particle strikes. The analysis techniques for the radiation particle strikes include: an approach to analytically determine the pulse width and the pulse shape of a radiation-induced voltage glitch in combinational circuits, a technique to model the dynamic stability of SRAMs, and a 3D device-level analysis of the radiation tolerance of voltage scaled circuits. Experimental results demonstrate that the proposed techniques for analyzing the effect of radiation particle strikes in combinational circuits and SRAMs are fast and accurate when compared with SPICE simulations. Therefore, these analysis approaches can be easily integrated in a VLSI design flow to analyze the radiation tolerance of ICs, to harden them early in the design flow. From 3D device-level analysis of the radiation tolerance of voltage scaled circuits, several nonintuitive observations are made and correspondingly, a set of guidelines are proposed, which are important to consider in order to realize radiation hardened circuits. In the first part of this monograph, two circuit level hardening approaches are also presented to harden combinational circuits against a radiation particle strike. These hardening approaches significantly improve the tolerance of combinational circuits against low and very high energy radiation particle strikes, respectively, with modest area and delay overheads.
The second part of this monograph addresses process variations. A technique is developed to perform sensitizable statistical timing analysis of a circuit, and thereby it improves the accuracy of timing analysis under process variations. Experimental results demonstrate that this technique is able to significantly reduce the pessimism due to two sources of inaccuracy, which plague current statistical static timing analysis (SSTA) tools. Two design approaches are also proposed to improve the process variation tolerance of combinational circuits and voltage level shifters (which are required in circuits with multiple interacting power supply domains), respectively. The variation tolerant design approach for combinational circuits significantly improves the resilience of these circuits to random process variations, with a reduction in the worst case delay and with a low area penalty. The proposed voltage level shifter is faster, requires lower dynamic power and area, has lower leakage currents, and is more tolerant to process variations, compared with the best known previous approach.

In summary, this monograph presents several analysis and design techniques which significantly augment the existing body of knowledge in the area of resilient VLSI circuit design.

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College Station, TX
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Rajesh Garg
Sunil P. Khatri
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Garg, R.
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