Contents

Preface v
Acknowledgments xi
List of Figures xix
List of Tables xxv

1. INTRODUCTION 1
   1.1 System-Design Challenges 1
   1.2 Abstraction Levels 3
      1.2.1 Y-Chart 3
      1.2.2 Processor-Level Behavioral Model 5
      1.2.3 Processor-level structural model 7
      1.2.4 Processor-level synthesis 10
      1.2.5 System-Level Behavioral Model 13
      1.2.6 System Structural Model 14
      1.2.7 System Synthesis 14
   1.3 System Design Methodology 18
      1.3.1 Missing semantics 20
      1.3.2 Model Algebra 21
   1.4 System-Level Models 23
   1.5 Platform Design 27
   1.6 System Design Tools 29
   1.7 Summary 32

2. SYSTEM DESIGN METHODOLOGIES 35
   2.1 Bottom-up Methodology 35
   2.2 Top-down Methodology 37
   2.3 Meet-in-the-middle Methodology 38
3.7 Summary 109

4. SYSTEM SYNTHESIS 113
   4.1 System Design Trends 114
   4.2 TLM Based Design 117
   4.3 Automatic TLM Generation 120
      4.3.1 Application Modeling 122
      4.3.2 Platform Definition 123
      4.3.3 Application to Platform Mapping 124
      4.3.4 TLM Based Performance Estimation 126
      4.3.5 TLM Semantics 130
   4.4 Automatic Mapping 132
      4.4.1 GSM Encoder Application 134
      4.4.2 Application Profiling 135
      4.4.3 Load Balancing Algorithm 138
      4.4.4 Longest Processing Time Algorithm 142
   4.5 Platform Synthesis 146
      4.5.1 Component data models 147
      4.5.2 Platform Generation Algorithm 148
      4.5.3 Cycle Accurate Model Generation 151
      4.5.4 Summary 152

5. SOFTWARE SYNTHESIS 155
   5.1 Preliminaries 156
      5.1.1 Target Languages for Embedded Systems 157
      5.1.2 RTOS 159
   5.2 Software Synthesis Overview 162
      5.2.1 Example Input TLM 164
      5.2.2 Target Architecture 166
   5.3 Code Generation 167
   5.4 Multi-Task Synthesis 173
      5.4.1 RTOS-based Multi-Tasking 173
      5.4.2 Interrupt-based Multi-Tasking 176
   5.5 Internal Communication 181
   5.6 External Communication 182
      5.6.1 Data Formatting 183
      5.6.2 Packetization 185
      5.6.3 Synchronization 186
      5.6.4 Media Access Control 191
5.7 Startup Code 193
5.8 Binary Image Generation 194
5.9 Execution 195
5.10 Summary 196

6. HARDWARE SYNTHESIS 199
6.1 RTL Architecture 201
6.2 Input Models 204
   6.2.1 C-code specification 204
   6.2.2 Control-Data Flow Graph specification 205
   6.2.3 Finite State Machine with Data specification 207
   6.2.4 RTL specification 208
   6.2.5 HDL specification 209
6.3 Estimation and Optimization 211
6.4 Register Sharing 216
6.5 Functional Unit Sharing 220
6.6 Connection Sharing 224
6.7 Register Merging 227
6.8 Chaining and Multi-Cycling 229
6.9 Functional-Unit Pipelining 232
6.10 Datapath Pipelining 235
6.11 Control and Datapath Pipelining 237
6.12 Scheduling 240
   6.12.1 RC scheduling 243
   6.12.2 TC scheduling 244
6.13 Interface Synthesis 248
6.14 Summary 253

7. VERIFICATION 255
7.1 Simulation Based Methods 257
   7.1.1 Stimulus Optimization 260
   7.1.2 Monitor Optimization 262
   7.1.3 SpeedUp Techniques 263
   7.1.4 Modeling Techniques 264
7.2 Formal Verification Methods 265
   7.2.1 Logic Equivalence Checking 266
   7.2.2 FSM Equivalence Checking 268
## Contents

7.2.3 Model Checking  270  
7.2.4 Theorem Proving  273  
7.2.5 Drawbacks of Formal Verification  275  
7.2.6 Improvements to Formal Verification Methods  275  
7.2.7 Semi-formal Methods: Symbolic Simulation  276  
7.3 Comparative Analysis of Verification Methods  276  
7.4 System Level Verification  278  
7.4.1 Formal Modeling  280  
7.4.2 Model Algebra  282  
7.4.3 Verification by Correct Refinement  283  
7.5 Summary  285  

8. EMBEDDED DESIGN PRACTICE  287  
8.1 System Level Design Tools  287  
8.1.1 Academic Tools  289  
8.1.2 Commercial Tools  296  
8.1.3 Outlook  299  
8.2 Embedded Software Design Tools  300  
8.2.1 Academic Tools  301  
8.2.2 Commercial Tools  303  
8.2.3 Outlook  305  
8.3 Hardware Design Tools  306  
8.3.1 Academic Tools  308  
8.3.2 Commercial Tools  314  
8.3.3 Outlook  319  
8.4 Case Study  319  
8.4.1 Embedded System Environment  320  
8.4.2 Design Driver: MP3 Decoder  324  
8.4.3 Results  327  
8.5 Summary  333  

References  335  

Index  349
Embedded System Design
Modeling, Synthesis and Verification
Gajski, D.D.; Abdi, S.; Gerstlauer, A.; Schirner, G.
2009, XXV, 352 p., Hardcover
ISBN: 978-1-4419-0503-1