1

Verilog —

A Tutorial Introduction

Getting Started
A Structural Description 2
Simulating the binaryToESeg Driver 4
Creating Ports For the Module 7
Creating a Testbench For a Module 8

Behavioral Modeling of Combinational Circuits 11
Procedural Models 12
Rules for Synthesizing Combinational Circuits 13

Procedural Modeling of Clocked Sequential Circuits 14
Modeling Finite State Machines 15
Rules for Synthesizing Sequential Systems 18
Non-Blocking Assignment (“<=”) 19

Module Hierarchy
The Counter 21
A Clock for the System 21
Tying the Whole Circuit Together 22
Tying Behavioral and Structural Models Together 25

Summary 27
Exercises 28

2

Logic Synthesis 35

Overview of Synthesis 35
Register-Transfer Level Systems 35
Disclaimer 36

Combinational Logic Using Gates and
Continuous Assign 37

Procedural Statements to Specify Combinational Logic 40
The Basics 40
Complications — Inferred Latches 42
Using Case Statements 43
Specifying Don’t Care Situations 44
Procedural Loop Constructs 46

Inferring Sequential Elements 48
  Latch Inferences 48
  Flip Flop Inferences 50
  Summary 52

Inferring Tri-State Devices 52

Describing Finite State Machines 53
  An Example of a Finite State Machine 53
  An Alternate Approach to FSM Specification 56

Finite State Machine and Datapath 58
  A Simple Computation 58
  A Datapath For Our System 58
  Details of the Functional Datapath Modules 60
  Wiring the Datapath Together 61
  Specifying the FSM 63

Summary on Logic Synthesis 66

Exercises 68

3

Behavioral Modeling 73

Process Model 73
If-Then-Else 75
  Where Does The ELSE Belong? 80
  The Conditional Operator 81

Loops 82
  Four Basic Loop Statements 82
  Exiting Loops on Exceptional Conditions 85

Multi-way Branching 86
  If-Else-If 86
  Case 86
  Comparison of Case and If-Else-If 89
  Casez and Casex 90

Functions and Tasks 91
  Tasks 93
  Functions 97
  A Structural View 100

Rules of Scope and Hierarchical Names 102
  Rules of Scope 102
  Hierarchical Names 105
Summary 106
Exercises 106

4 Concurrent Processes 109

Concurrent Processes 109
Events 111
  Event Control Statement 112
  Named Events 113
The Wait Statement 116
  A Complete Producer-Consumer Handshake 117
  Comparison of the Wait and While Statements 120
  Comparison of Wait and Event Control Statements 121
A Concurrent Process Example 122
A Simple Pipelined Processor 128
  The Basic Processor 128
  Synchronization Between Pipestages 130
Disabling Named Blocks 132
Intra-Assignment Control and Timing Events 134
Procedural Continuous Assignment 136
Sequential and Parallel Blocks 138
Exercises 140

5 Module Hierarchy 143

Module Instantiation and Port Specifications 143
Parameters 146
Arrays of Instances 150
Generate Blocks 151
Exercises 154
8

Advanced Timing

Verilog Timing Models 211
Basic Model of a Simulator 214
Gate Level Simulation 215
Towards a More General Model 215
Scheduling Behavioral Models 218
Non-Deterministic Behavior of the Simulation Algorithm 220
Near a Black Hole 221
It's a Concurrent Language 223
Non-Blocking Procedural Assignments 226
Contrasting Blocking and Non-Blocking Assignments 226
Prevalent Usage of the Non-Blocking Assignment 227
Extending the Event-Driven Scheduling Algorithm 228
Illustrating Non-Blocking Assignments 231
Summary 233
Exercises 234

9

User-Defined Primitives 239

Combinational Primitives 240
Basic Features of User-Defined Primitives 240
Describing Combinational Logic Circuits 242
Sequential Primitives 243
Level-Sensitive Primitives 244
Edge-Sensitive Primitives 244
Shorthand Notation 246
Mixed Level- and Edge-Sensitive Primitives 246
Summary 249
Exercises 249
10 Switch Level Modeling

A Dynamic MOS Shift Register Example 251
Switch Level Modeling 256
Strength Modeling 256
Strength Definitions 259
An Example Using Strengths 260
Resistive MOS Gates 262
Ambiguous Strengths 263
Illustrations of Ambiguous Strengths 264
The Underlying Calculations 265
The miniSim Example 270
Overview 270
The miniSim Source 271
Simulation Results 280
Summary 281
Exercises 281

11 Projects

Modeling Power Dissipation 283
Modeling Power Dissipation 284
What to do 284
Steps 285
A Floppy Disk Controller 286
Introduction 286
Disk Format 287
Function Descriptions 288
Reality Sets In... 291
Everything You Always Wanted to Know about CRC's 291
Supporting Verilog Modules 292

Appendix A: Tutorial Questions and Discussion 293
Structural Descriptions 293
Testbench Modules 303
Combinational Circuits Using always 303
<table>
<thead>
<tr>
<th>Appendix B: Lexical Conventions</th>
<th>309</th>
</tr>
</thead>
<tbody>
<tr>
<td>White Space and Comments</td>
<td>309</td>
</tr>
<tr>
<td>Operators</td>
<td>310</td>
</tr>
<tr>
<td>Numbers</td>
<td>310</td>
</tr>
<tr>
<td>Strings</td>
<td>311</td>
</tr>
<tr>
<td>Identifiers, System Names, and Keywords</td>
<td>312</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Appendix C: Verilog Operators</th>
<th>315</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table of Operators</td>
<td>315</td>
</tr>
<tr>
<td>Operator Precedence</td>
<td>320</td>
</tr>
<tr>
<td>Operator Truth Tables</td>
<td>321</td>
</tr>
<tr>
<td>Expression Bit Lengths</td>
<td>322</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Appendix D: Verilog Gate Types</th>
<th>323</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Gates</td>
<td>323</td>
</tr>
<tr>
<td>BUF and NOT Gates</td>
<td>325</td>
</tr>
<tr>
<td>BUFIF and NOTIF Gates</td>
<td>326</td>
</tr>
<tr>
<td>MOS Gates</td>
<td>327</td>
</tr>
<tr>
<td>Bidirectional Gates</td>
<td>328</td>
</tr>
<tr>
<td>CMOS Gates</td>
<td>328</td>
</tr>
<tr>
<td>Pullup and Pulldown Gates</td>
<td>328</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Appendix E: Registers, Memories, Integers, and Time</th>
<th>329</th>
</tr>
</thead>
<tbody>
<tr>
<td>Registers</td>
<td>329</td>
</tr>
<tr>
<td>Memories</td>
<td>330</td>
</tr>
<tr>
<td>Integers and Times</td>
<td>331</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Appendix F: System Tasks and Functions</th>
<th>333</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display and Write Tasks</td>
<td>333</td>
</tr>
<tr>
<td>Continuous Monitoring</td>
<td>334</td>
</tr>
<tr>
<td>Strobed Monitoring</td>
<td>335</td>
</tr>
<tr>
<td>File Output</td>
<td>335</td>
</tr>
<tr>
<td>Simulation Time</td>
<td>336</td>
</tr>
<tr>
<td>Stop and Finish</td>
<td>336</td>
</tr>
<tr>
<td>Random</td>
<td>336</td>
</tr>
<tr>
<td>Reading Data From Disk Files</td>
<td>337</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Appendix G: Formal Syntax Definition</th>
<th>339</th>
</tr>
</thead>
</table>
Source text 343
Declarations 346
Primitive Instances 351
Module and generated instantiation 353
UDP declaration and instantiation 355
Behavioral statements 355
Specify section 359
Expressions 365
General 370

Index 373
The Verilog® Hardware Description Language
Thomas, D.; Moorby, P.
2002, XXII, 386 p. With online files/update., Softcover
ISBN: 978-0-387-84930-0