the design to consume significantly more power during test than it would during nor-
mal operation. If the design has only been packaged assuming functional power dissi-
pation numbers then thermal failure of both the design and package at test can result.
In addition, this increased power consumption in the core can lead to significant volt-
age drop in the power distribution network which in turn leads to functional failure. It
is therefore necessary to consider the requirements of both the functional and test
modes of the design when implementing voltage scaling.

When performing manufacturing test on designs implemented in very small geomet-
ries (90/65/45 nm) it is necessary to use a variety of test models and test strategies.
Specifically, testing the design with stuck-at faults models now needs to be compli-
mented with transition fault delay testing. Delay fault testing is particularly suscepti-
ble to changes in the voltage and frequency at which a design operates. Similarly,
path based testing is also dependent upon the voltage at which the design is being
operated. As will be discussed later in this chapter, the critical path of a voltage scaled
design is not the same path at each voltage level at which the design operates. Each
performance level supported by the design may well have a unique critical path. Each
of these paths needs to be tested during at-speed test in a manufacturing test environ-
ment.

However, as we reduce the supply voltages at which we test our design, delay behav-
ior changes dramatically. In particular, weak circuit elements and defective circuit
elements do not behave in the same way. In addition, the tester environment differs
from the system environment in noise content, heat dissipation and pin load. As a
result, care needs to be taken to distinguish between correct behavior and defective
behavior. In many cases, final decisions on correct timing and voltage levels will need
to wait until silicon is available.

Automating the manufacturing test process will require performing stuck-at fault test-
ing and delay fault testing at several operating voltages, and also may involve both
nominal and high temperature test. Developing the appropriate mix of tests in order to
guarantee sufficient quality at reasonable cost is a complex problem. Different trade-
offs between test time and coverage will apply to different products.
Low Power Methodology Manual
For System-on-Chip Design
Flynn, D.; Aitken, R.; Gibbons, A.; Shi, K.
2007, XVI, 300 p., Hardcover