Chapter 2
Continuous-Time Delta-Sigma Modulator

This chapter starts with a brief explanation of the operation of an ideal single-loop continuous-time delta-sigma (CTΔΣ) modulator and describes its major building blocks, i.e. the loop filter, quantizer and digital-to-analog converter (DAC). In Sect. 2.2, we introduce the system-level non-idealities that limit the performance of such a modulator. Finally, we will illustrate the effect of system-level non-idealities on the key performance metrics of the modulator: its signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and sampling speed ($f_s$).

2.1 Ideal Delta-Sigma Modulator

2.1.1 System Overview

A basic model of a single-loop delta-sigma modulator (ΔΣM) is shown in Fig. 2.1a. It has three main building blocks: a quantizer, a DAC and a loop filter. Although, a ΔΣM is a non-linear feedback system, it can be approximated by a linear model (Fig. 2.1b) in order to develop a basic understanding of its behavior. The quantizer can be modeled as an error source which has a white noise spectrum. The DAC can be modeled as a unity gain stage, and the transfer function of the ΔΣM is expressed as:

$$Y(s) = X(s) \cdot \frac{H_L(s)}{1 + H_L(s)} + E_Q(s) \cdot \frac{1}{1 + H_L(s)}$$

$$= X(s) \cdot STF(s) + E_Q(s) \cdot NTF(s),$$

(2.1)

where $X$ is the input signal, $E_Q$ is the quantization noise, and $H_L$ is the transfer function of the loop filter. The input signal and quantization noise are subject to
different transfer functions, which are known as the signal transfer function (STF) and the noise transfer function (NTF), respectively. Figure 2.2 presents the STF and NTF of a 3rd order feedforward ΔΣM. When $H_L$ consists of a cascade of integrators, then the quantization noise is high-pass filtered and is thus attenuated,
or in other words, shaped in the band of interest due to the gain provided by the loop filter. On the other hand, the input signals located in the band of interest are processed without any attenuation.

In a CTΔΣ modulator, the sampling takes place at the output of the loop filter. These sampled values can be obtained from a discrete-time equivalent ($H_{L,dt}(z)$) of the continuous-time loop filter ($H_L(s)$), which can be obtained by using the impulse-invariant transformation [1]. This will be explained in more detail in Sect. 2.2.3.

One of the most important advantages of a CTΔΣ modulator is its inherent anti-alias filtering (AAF). In a Nyquist analog-to-digital converter (ADC), signals at $n \cdot f_s \pm f_b$ alias to $f_b < BW$ due to the sampling and cannot be distinguished from the signals present at $f < BW$. In a CTΔΣ modulator, however, the sampling takes place at the output of the loop filter and so signals which might alias are low-pass filtered by the loop filter. Therefore, the inherent AAF simplifies the filtering required in the analog front end. The aliasing component of a signal with frequency ($\omega = 2\pi (n \cdot f_s \pm f_b)$) is scaled by the response of AAF, which is expressed for the single-loop $\Delta \Sigma M$ as [2]:

$$AAF(\omega) = \frac{H_L(j\omega)}{H_{L,dt}(e^{j\omega T_s})},$$

(2.2)

where $H_L$, $H_{L,dt}$ are the continuous-time and discrete-time equivalent of the loop filter, respectively. Figure 2.3 shows the gain response of the 3rd order modulator (Sect. 2.1.4) with AAF around $(f_s \pm f_b)$. For higher-order modulators, a more aggressive AAF roll-off can be achieved [3].

As mentioned before, a $\Delta \Sigma M$ is a high-order feedback system and so it is not necessarily stable. A complete analysis of its stability is not trivial since the
quantizer is a non-linear element. In most practical cases, the stability of a $\Delta\Sigma M$ is verified by computer simulations [4, 5]. However, the building blocks of a modulator can be modeled to a certain extent, which reveals the link between its stability and the characteristics of each building block. Then, it is possible to establish a basic understanding of the stability of a $\Delta\Sigma M$ and analyze how each building block effects the operation of the modulator. Therefore, in the following sub-sections, the main building blocks of an ideal single loop $\Delta\Sigma M$ are described in more detail.

### 2.1.2 Quantizer

The quantizer converts the output of the loop filter to digital, and is the only non-linear element of the ideal modulator. The linearized transfer function can be expressed as:

$$Y(n \cdot T_s) = G \cdot X(n \cdot T_s) + E_Q(n \cdot T_s),$$

(2.3)

where $G$ is the gain of the quantizer and $E_Q$ is the quantization error. An example of the transfer function of a 2 bit quantizer with a unit-step size ($\Delta = 1$) is shown in Fig. 2.4a. The maximum input amplitude is defined as $A_m = 2^{B-1}$ where $B$ is the number of bits of the quantizer. For an input signal lower than $A_m$, the quantizer is not overloaded and the quantization error is bounded between $\pm \Delta / 2$ (Fig. 2.4b). For a uniformly distributed quantization noise, its power is expressed as [4]:

$$E_{Q,\text{rms}}^2 = \Delta^2 / 12.$$  

(2.4)

For input frequencies that are a rational fraction of the sampling frequency, a single-bit quantizer exhibits phase uncertainty [6]. Figure 2.5 shows the output of a single-bit quantizer (indicated by the arrows) for an input signal at $f_s / 4$. If the signal crosses zero between two consecutive samples of the quantizer, the output of the quantizer will only toggle at the next sampling instance. For an input signal at $f_s / 4$, the single-bit quantizer has a $\pm \pi / 4$ phase uncertainty. In other words, shifting the input signal by $\pm \pi / 4$ results in exactly the same output. Therefore, the simple gain model of the quantizer can be extended to accommodate the phase uncertainty. The linear gain ($G$) in (2.3) is replaced by $G \cdot e^{s\theta}$, where $\theta$ is the phase uncertainty.

The non-linear behavior of the quantizer has a significant effect on the stability of the modulator. The phase uncertainty of a single-bit $\Delta\Sigma M$ causes idle-patterns at the output of the modulator, which can cause instability. During the design of a single-bit modulator, therefore, the phase uncertainty must be taken into account to ensure a stable modulator. This effect is less dominant in a multi-bit quantizer. The phase uncertainty of a quantizer can be neglected for $B > 3$ [7].

In addition to the phase uncertainty, the uniformly distributed quantization noise assumption does not hold for a noiseless sine-wave input. The quantization error and the input signal will be highly correlated and harmonic distortion will be present
at the output of the quantizer. This effect is especially dominant in a single-bit quantizer. For example, for an input signal at $f_{in} \ll f_s$, the output of the quantizer can be approximated as a square wave at $f_{in}$ which has odd harmonics of the input frequency. A detailed analysis of the nonlinearity of an ideal quantizer is presented in Appendix B.

Figure 2.6 shows the harmonic distortion and intermodulation of an ideal quantizer. For a 3rd harmonic distortion (HD$_3$) simulation, the input signal is set to $f_{in} = 0.15 \times f_s$, and for an IM$_3$ simulation the input is set to $f_{in} \pm \Delta f$ where $\Delta f = f_s/32$ for a two-tone input signal. The maximum resolution of the quantizer is set to 5 bits because higher resolution is not of practical interest. The simulation results are in agreement with the theoretical calculations (B.4, B.5).
Fig. 2.5 Phase uncertainty of a single-bit quantizer for a sinewave at $f_s/4$

Fig. 2.6 Signal-to-noise ratio (SNR), 3rd order harmonic distortion (HD$_3$), and 3rd order intermodulation (IM$_3$) of a quantizer
As the resolution of the quantizer increases the $HD_3$ and $IM_3$ improve. As a result, the nonlinearity of the quantizer can be neglected for $B > 3$ since the gain of the loop filter will further suppress these tones. Moreover, the nonlinearity of other blocks is often higher than the nonlinearity of the multi-bit quantizer assuming that the slices of the quantizer do not have any mismatch.

On the other hand, there is always some noise at the input of the quantizer in a practical implementation. The additional noise $de$-$correlates$ the distortion tones generated by the quantizer and improves the $HD_3$ and $IM_3$ [8]. To illustrate this effect, a uniformly distributed noise with an amplitude of $1\,LSB$ is added at the input of the quantizer and the input amplitude is reduced to prevent the overloading of the quantizer. The simulation results are shown in Fig. 2.7. The SNR diminishes due to the additional noise, but $HD_3$ and $IM_3$ improve by more than 10 dB. Therefore, a quantizer will exhibit fewer distortion tones when used in a $\Delta \Sigma M$ due to the thermal noise present in the modulator.

Furthermore, the harmonics introduced by the quantizer are attenuated by the loop gain provided by the $\Delta \Sigma M$. However, the tones introduced by a single-bit quantizer cannot be ignored in low-order modulators. As the resolution of the quantizer increases, the $HD_3$ and $IM_3$ introduced by the quantizer become less dominant (Sect. 2.2).

### 2.1.3 DAC

The DAC is often the only block placed in the feedback of the modulator. In most cases, it uses the same number of levels as the quantizer and it converts the output of the quantizer into an analog signal by using voltage or current sources connected
to the input of the loop filter. Furthermore, it introduces a zero-order hold (ZOH) function to the feedback of the modulator. The DAC output waveform can have different shapes depending on the implementation requirements. Two commonly used DAC waveforms which are suitable for high-speed ΔΣMs are illustrated in Fig. 2.8. A non-return-to-zero (NRZ) DAC holds the value of the digital data for one clock period \((T_s)\), whereas a return-to-zero (RZ) DAC uses only a fraction of the clock period. To analyze the stability of the modulator, the transfer function of the DAC waveforms (Fig. 2.8) can be expressed as:

\[
H_{DAC, NRZ}(s) = \frac{1 - e^{-sT_s}}{s},
\]

\[
H_{DAC, RZ}(s) = \frac{e^{-s(t_d)} \cdot (1 - e^{-st_p})}{s},
\]

where \(t_d\) is the delay and \(t_p\) is the pulse width of the RZ DAC. The DAC introduces a frequency-dependent amplitude and phase response as shown in Fig. 2.9. The phase shift of an NRZ DAC is \(90^\circ\) at \(f_s/2\), which must be taken into account when considering the stability of the modulator.

### 2.1.4 Loop Filter

The loop filter provides gain for the modulator which attenuates the quantization errors in the band of interest. It can usually be approximated as being a cascade of ideal integrator stages. Thus the transfer function of an Nth order loop filter can be expressed as:

\[
H_L(s) = \left(\frac{1}{s}\right)^N.
\]

A higher-order loop filter achieves more aggressive noise shaping but at the cost of degrading the stability. An often-mentioned stability criterion for a ΔΣM is that it generates bounded outputs for bounded input signals [4, 5, 9].
For a zero-input signal, the output of the multi-bit modulator (Fig. 2.1a) will be \((\ldots, +\text{LSB}, -\text{LSB}, +\text{LSB}, -\text{LSB}, \ldots)\), the average value of the output will be zero, and the frequency of oscillation will be \(f_s/2\). In other words, a stable \(\Delta\Sigma M\) exhibits tones at \(f_s/2\) for a bounded input signal.

To achieve controlled oscillations at \(f_s/2\), the gain and phase of the closed-loop transfer function of the modulator at \(f_s/2\) must be “1” and \(2/\pi\)”, respectively which is also known as the Barkhausen stability criterion. The gain and phase response of the closed-loop transfer function of the modulator at \(f_s/2\) can be expressed as:

\[
|G(s) \cdot H_{\text{DAC}}(s) \cdot H_L(s)|_{s=j\pi f_s} = 1
\]

\[
\angle (G(s) \cdot H_{\text{DAC}}(s) \cdot H_L(s))|_{s=j\pi f_s} = 2\pi,
\]

where \(G\) and \(H_{\text{DAC}}\) are the transfer functions of the quantizer and DAC, respectively. For example, a 1st order \(\Delta\Sigma M\) is inherently stable for a bounded input signal and satisfies the gain and phase requirement defined by (2.8). The signal dependent gain of the quantizer guarantees a closed-loop gain of “1” [4]. Moreover, the phase shift of the closed-loop is 360°, where the 1st order loop filter, NRZ DAC (Sect. 2.1.3), and the sign inversion at the summation contribute 90°, 90°, and 180° of the phase shift, respectively. For higher-order modulators, the phase shift of the loop filter increases to \((N \cdot \pi)/2\). Therefore, a solution to (2.8) does not exist and
the modulator is unstable. To overcome this limitation, \((N - 1)\) zeros are introduced to the transfer function, which can be expressed as:

\[
H_L(s) = \frac{\prod_{k=1}^{N-1}(s + s_k)}{s^N}.
\]  

(2.9)

This can be achieved using a feedforward loop filter as shown in Fig. 2.10a. This loop filter architecture requires coefficients \((a_1, a_2, \ldots, a_N)\) and a summation node at the output of the loop filter. The STF of a modulator with a feedforward loop filter has an out-of-band peaking as shown in Fig. 2.11. Indeed, the modulator does amplify certain signals, which can be out-of-band blockers or interferers, therefore the system might require filtering before the modulator. On the other hand, the other STF shown in Fig. 2.11 does not exhibit any peaking. In this case, the loop filter employs the feedback architecture shown in Fig. 2.10b. However, the feedback loop filter requires \(N \cdot DAC s\) to implement the coefficients \((a_1, a_2, \ldots, a_N)\), which increases the system complexity. The output of the modulator is fed back to the output of each integrator stage. Therefore, the replica of the input signal is present at each integrator’s output, which requires an amplifier that can generate a large output swing.

In practice, placing the loop filter zeros close to the poles reduces the effective gain of the loop filter so that \(H_L(s)\) can be approximated as a 1\(^{st}\) order loop filter for frequencies around \(0.5 \times f_s\). However, the signal-to-quantization noise ratio (SQNR) of the modulator is especially compromised for low oversampling ratios. In order to define a possible location of the zeros, the approach for Butterworth filters can be used in which the poles of filter is distributed evenly around the
Left-Hand Plane (LHP) unit circle. Therefore, following (2.10), the zero locations can be expressed as:

\[ s_k = -\omega_z e^{j\pi(2k+n-1)} \quad \text{where} \quad k = 1, 2, 3, \ldots, N - 1, \]  

where \( \omega_z \) defines the location of the zero. By choosing a low enough \( \omega_z \), a phase shift close to \( 90^\circ \) at \( f_s/2 \) can be achieved without degrading the gain in the signal band too much. Figure 2.12 shows the bode plot of a 3rd order feedforward loop filter which has Butterworth aligned zeros, and \( \omega_z \) set to 0.025 \( \times \) \( f_s \), which results in a 96\(^\circ\) phase shift. However, this condition is not sufficient to guarantee a stable operation, therefore system-level simulations are still required to verify the stability of the modulator.

### 2.2 System-Level Non-idealities

This section discusses the system-level non-idealities in a \( \Delta \Sigma \)M such as: noise, nonlinearity, metastability and excess loop delay (ELD). Noise is an unwanted random fluctuation, which is common to all electronic circuits. Circuit noise limits the SNR. Nonlinearity is a behaviour of modulator’s building block, in which the output signal does not follow the input in direct proportion. The nonlinearity of the blocks degrades the SFDR. ELD is the latency between the quantizer clock edge and the time when a change in the output of the DAC occurs [10–12]. The ELD can cause an unstable modulator, and in this case, the output of the modulator will not
follow the input signal. Metastability exits in digital latches, in which the output of the latch persists at an unstable state for an unknown duration. The metastable state is not a valid digital state (i.e. “1”, “0”), therefore introduces additional noise and reduces the SNR.

### 2.2.1 Noise

In a theoretical $\Delta \Sigma M$, the quantization error fundamentally defines the maximum achievable SNR. To improve the SNR, the NTF of the modulator is optimized by carefully choosing system-level design parameters such as the order of the loop filter, the resolution of the quantizer, and the oversampling ratio (OSR). However, the building blocks of the modulator also introduce noise and degrade the SNR. Therefore, in an optimal ADC design (thermal noise limited), the quantization noise is set to at least 10 dB lower than the thermal noise.

The thermal noise of the building blocks sets a practical limit on the maximum achievable SNR [13, 14]. The transfer function of the noise sources present in the modulator (Fig. 2.13) can be expressed as:

$$Y^2 = \left(n_{DAC}^2 + n_{LF}^2\right) \cdot \left(\frac{H_L}{1 + H_L}\right)^2 + n_Q^2 \cdot \left(\frac{1}{1 + H_L}\right)^2,$$

(2.11)
Fig. 2.13 Noise sources in a single-loop CTΔΣ modulator

\[ X(t) \rightarrow DAC \rightarrow Loop \ Filter \rightarrow Quantizer \rightarrow Y(n) \]

where \( n^2_{DAC} \) is the thermal noise of the DAC, \( n^2_{LF} \) is the input referred thermal noise of the loop filter and \( n^2_{Q} \) is the thermal noise of the quantizer referred to its input. The loop filter and the DAC are connected to the input of the ADC, therefore they are the most dominant noise sources. The loop filter mainly introduces thermal noise. In wide bandwidth modulators, the focus of this book, offset and \( 1/f \) noise of the CMOS transistors can be neglected. Another unimportant noise source is the thermal noise of the quantizer \( (n^2_{Q}) \) because it is also attenuated by the NTF. The decimation filter suppresses the noise that is outside of the signal bandwidth.

In addition to the thermal noise, the phase noise of the sampling clock decreases the SNR since the ΔΣM is a sampled system. Due to the noisy sampling clock, the edges of the DAC output are not well-defined. This effect can be quantified by the signal-to-jitter-noise-ratio (SJNR), which is the ratio of the signal power to the jitter noise power at the output of the modulator. In most cases, the clock of an ADC is specified in terms of root-mean-square (RMS) jitter rather than in terms of phase noise as is commonly done in oscillators or clock sources. Figure 2.14a illustrates the phase noise of an oscillator, from which the jitter specifications can be derived. The phase noise increases for frequencies less than the noise corner. For frequencies
beyond the noise corner, the oscillator noise spectrum is white, and is determined by the noise of the output buffers of the oscillator. The RMS jitter can be estimated as [15]:

$$Jitter(RMS) = \frac{\sqrt{2 \cdot 10^{IPN/10}}}{2 \pi \cdot f_{clk}},$$

(2.12)

where IPN is the integrated phase noise from \( f_{start} \) to \( f_{stop} \). The \( f_{start} \) depends on the spectral resolution required by the application. In practice, \( f_{start} \) as low as 10–100 Hz is common and \( f_{stop} \) is set to the sampling frequency of the ADC assuming that the bandwidth of the clock input is limited to the sampling frequency. For a \( \Delta \Sigma M \), \( f_{stop} \) is set to the oversampled clock frequency.

The noise due to the clock jitter depends both on the implementation of the feedback DAC and the clock source. If we assume that the DAC is implemented with NRZ pulses, the phase noise will distort the DAC pulse shape (Fig. 2.14b). An NRZ DAC is advantageous because it only switches when the data toggles. Therefore, it introduces less noise compared to an RZ DAC [16].

Since the DAC is connected to the input of the ADC, the clock jitter-induced errors also appear at the output of the ADC without any filtering. For a \( \Delta \Sigma M \) aiming at GHz sampling frequencies, the effect of phase noise can limit the SNR. The phase noise of the clock convolves with the input signal, and the ADC’s selectivity will be limited by the close-in phase noise of the oscillator. On the other hand, the white noise of the oscillator mixes with the quantization noise and down-converts it into the baseband. This increases the in-band noise and thus limits the dynamic range of the ADC [17].

At the system level, the effect of clock jitter can be simulated in two steps. First of all, a square-wave clock signal is generated based on the phase noise model of a clock source in MATLAB. The phase noise spectrum of the clock source is shown in Fig. 2.15. Then the behavioral model of a 3rd order \( \Delta \Sigma M \) with a 4-bit quantizer is simulated in Simulink. The multi-bit DAC of the modulator is triggered with the clock source generated in MATLAB; the effect of clock jitter is shown in Fig. 2.16. As explained before, the close-in phase noise of the clock can be observed around the input signal, and the white-noise of the clock increases the in-band noise floor.

### 2.2.2 Non-linearity

As explained in Sect. 2.1.2, the quantizer is the only inherently non-linear building block of the modulator. A single-bit quantizer demonstrates the highest non-linearity, although when placed in a \( \Delta \Sigma M \), the non-linearity of the quantizer is suppressed by the gain of the loop filter. Figure 2.17 shows an FFT of the simulated output of a 3rd order single-bit \( \Delta \Sigma \) ADC with a full scale input signal. Especially, \( HD_3 \) is present at the output of the modulator. To further reduce and de-correlate \( HD_3 \), additional dithering can be applied to the input of the quantizer [4], however, reducing maximum stable input amplitude of the modulator.
2.2 System-Level Non-idealities

Fig. 2.15 The single side-band spectrum of a non-ideal sampling clock

Fig. 2.16 The output spectrum of the 3rd order CTΔΣ modulator with a non-ideal sampling clock (FFT size is $2^{15}$ pts)
A multi-bit quantizer is intrinsically more linear than a single-bit comparator. A ΔΣM with a multi-bit quantizer does not generate visible harmonic distortion (HD) tones and can also achieve more aggressive noise shaping. Such multi-bit modulators usually employ multi-bit DACs. In a practical implementation, each DAC unit will deviate from its nominal value due to the mismatch introduced by the process variation, so the multi-bit DAC introduces distortion. The standard deviation of a DAC unit is usually in the order of 0.1–10% in the current fabrication processes. Figure 2.18 shows an FFT of the simulated output of a 4-bit 3rd order ΔΣ ADC with $\sigma_{IDAC}/I_{DAC} = 0.2\%$. It can be seen that DAC mismatch limits the linearity of a multi-bit ΔΣM. However, this limitation can be overcome by various techniques such as: dynamic element matching (DEM) and calibration of DAC current sources [18–21], but these techniques increase the complexity of the system.

### 2.2.3 Excess Loop Delay

As explained in the previous section, the stability of a ΔΣM relies on the amplitude and phase response of the loop. However, in a real implementation, the building blocks also introduce ELD, which is defined as the time delay between the quantizer clock edge and the time when a change in the output of the DAC occurs [10–12]. ELD is basically caused by the limited speed of the transistors used to implement the
quantizer and the DAC of a \( \Delta \Sigma \)M. As shown in Fig. 2.19a, it can be modeled as a discrete time delay \( z^{-r_p} \). As the ELD increases, the phase shift in the loop increases, which ultimately causes the \( \Delta \Sigma \)M to become unstable.

To illustrate the effect of ELD, the amplitude and phase response of the loop filter of a 3\(^{rd}\) order 4-bit \( \Delta \Sigma \)M with a one-clock period of ELD is shown in Fig. 2.20. The amplitude and phase response of the DAC and the summation node at the input of the modulator have been neglected. The amplitude response of the loop filter is not affected, but the phase response of the loop filter (designed to achieve a phase shift of 90\(^{\circ}\)) is degraded due to the ELD. From our previous analysis, we can conclude that a modulator with a one-clock cycle delay is unstable. The exact relation between the stability and the ELD depends on the design of the modulator.

As shown in Fig. 2.21, the SQNR of the modulator stays flat up to 0.3 \( \times T_s \) ELD. However, the modulator is not stable beyond this value. An in-depth study of the simulation results reveals that non-zero ELD causes the output swing of the integrators to increase beyond their designed values. Furthermore, any clipping in a practical implementation, which is especially a problem at the summation node, can push the modulator into instability for much smaller values of ELD.

To compensate the increase in phase shift due to ELD and recover from an unstable mode of operation, the modulator requires an additional zero that will bypass the loop filter at \( f_s/2 \). This is achieved by introducing a feedback DAC with a coefficient \((c)\) around the quantizer as shown in Fig. 2.19b [11, 22]. Since the calculation of the loop-filter coefficients is straightforward in the \( Z \)-domain, the continuous-time loop filter \((H_L(s))\) is transformed to its discrete-time equivalent

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**Fig. 2.18** The harmonic tones due to the mismatch of a multi-bit DAC (FFT size is \(2^{17} \text{ pts}\))
In order to find the discrete-time (DT) equivalent of the continuous-time (CT) loop filter, the impulse-invariant transformation is preferred since we assume that two modulators are equivalent, for a given input signal, if their loop filter generates the same outputs at the sampling moments of their quantizers \([23]\). Mapping of a CT loop filter to a DT equivalent is only valid for \( f \ll f_s \). However, for the following analysis \((2.16-2.18)\), we rely on \((2.13)\) which maps the sampled instances of the CT loop filter into its discrete-time equivalent.

In general, the main motivation of the ELD compensation technique is to preserve the original NTF of the modulator and thus the stability of the modulator. Therefore, a new loop filter \((H_{L,dt}(z))\) is required to keep the same NTF. So from the viewpoint of stability, the new loop filter \((H_{LD,dt}(z))\) can be determined from:

\[
H_{LD,dt}(z) = H_{L,dt}(z)z^{-T_p} - c,
\]  

\[(2.14)\]
where the feedback DAC has an NRZ waveform. The continuous-time equivalent of the new loop filter is then calculated by applying the inverse of the impulse-invariant transformation (2.13).
Assuming both the $H_{L, dt}(z)$ and $H_{L, D, dt}(z)$ are implemented by using the same filter order, ELD up to one clock cycle delay can be compensated by using (2.14) and the modulator achieves the same SQNR and NTF. For the ELD more than one clock cycle, a solution to (2.14) does not exist since the $H_{L, dt}(z)$ and $H_{L, D, dt}(z)$ have the same filter architecture. A $\Delta\Sigma$M which uses the ELD compensation technique shown in Fig. 2.19b is unstable for ELD more than one clock cycle.

For example, a 2nd order modulator with an ideal $NTF(z) = (1 - z^{-1})^2$ has a discrete-time equivalent loop filter which is:

$$H_{L, dt}(z) = \frac{1 - NTF(z)}{NTF(z)}$$

$$\frac{a_1 z^{-1} + a_2 z^{-2}}{1 - 2z^{-1} + z^{-2}} = \frac{2z^{-1} - z^{-2}}{1 - 2z^{-1} + z^{-2}}$$

$$a_1 = 2$$
$$a_2 = -1$$

(2.15)

The continuous-time equivalent of the loop filter with a NRZ DAC pulse can be determined by inverting (2.13):

$$H_L(s) = \frac{1.5}{s} + \frac{1}{s^2}. \quad (2.16)$$

Assuming there is one clock cycle delay ($z^{c^p} = z^1$), the new loop filter ($H_{L, D, dt}(z)$) will have the same structure as the original loop filter and following (2.14):

$$H_{L, D, dt}(z) = H_{L, dt}(z) \cdot z^1 - c$$

$$\frac{a_{1d} z^{-1} - a_{2d} z^{-2}}{1 - 2z^{-1} + z^{-2}} = \frac{a_1 z^{-1} - a_2 z^{-2}}{1 - 2z^{-1} + z^{-2}} \cdot z^1 - c$$

$$a_{1d} = 2a_1 + a_2 = 3$$
$$a_{2d} = a_1 = 2$$
$$c = a_1 = 2$$

(2.17)

The continuous-time equivalent of the new loop filter with a NRZ DAC pulse can be determined by inverting (2.13):

$$H_{LD}(s) = \frac{2.5}{s} + \frac{1}{s^2}. \quad (2.18)$$
Even though the modulator has the same NTF, the STF of the modulator is modified since there exists a new loop filter ($H_{LD}(s)$). As a result, the new STF of the modulator is expressed as:

$$\text{STF}_{D}(s) |_{\omega = \omega_0} = H_{LD}(s) |_{\omega = \omega_0} \cdot \text{NTF}(z) |_{z = e^{j\omega T_s}}.$$  \hspace{1cm} (2.19)

In particular, the peaking in the STF of the \( \Delta \Sigma \)M increases and the center frequency of the peaking shifts to a higher frequency. This will be explained in more detail in Sect. 3.1.3.

In addition to the ELD compensation technique shown in Fig. 2.19b, an attractive solution that can be implemented in CMOS processes is to compensate for the loop delay in the digital domain as shown in Fig. 2.22 [24]. However, extra hardware is required which introduces additional delay and further pushes the digital circuitry to its limits. A part of the dynamic range (DR) is used for compensating the delay in the digital domain [25]. Considering those drawbacks, an analog delay compensation method is preferred in designs which aim for a high sampling speed.

To maintain the NTF and satisfy the stability requirements of the modulator, the summation node presented in Fig. 2.19b should not introduce additional ELD. A summation node can be implemented in analog domain by the use of active amplifiers. An interesting modification to the analog ELD compensation is to place the summation node at the input of the last integrator. A possible implementation of this technique is shown in Fig. 2.23. By using this technique, the additional summation node that is required for the ELD compensation is not necessary anymore. However, the input to the coefficient ($c$) must be differentiated in the digital domain ($1- z^{-0.5}$) to implement a summation node [26]. To preserve stability, the amplifier that implements the last integrator must have a wide bandwidth for a minimal delay [25], as well as high gain for reducing the variation of the loop-filter coefficients over process, voltage, and temperature (PVT). These stringent requirements result in a power-hungry summing amplifier.

The ELD compensation techniques described above can compensate for up to a one-clock period delay without losing any SQNR. In the case of larger ELD, the maximum input amplitude of the modulator will decrease, which will result in a
2.2.4 Metastability

To achieve very high sampling rates, a flash ADC is often employed as the quantizer of a $\Delta \Sigma$M. An N-bit flash ADC employs $2^N$ comparators. Each comparator employs a digital latch which suffers from metastability errors for very small input loss in DR and eventually cause the modulator to become unstable. To overcome this limitation, the quantizer can be bypassed by an auxiliary fast loop which is implemented by a sample-and-hold (S&H) and a scaling coefficient ($c$) [27] shown in Fig. 2.24. The auxiliary fast loop measures the output of the loop filter and compensates the phase shift due to more than one-clock period of ELD. This approach can compensate for $1.5T_s$ of ELD at the cost of reducing the order of noise shaping by one[27].
2.2 System-Level Non-idealities

Fig. 2.25  Block diagram of the comparator

\[ \text{signals } [28, 29]. \text{ As a result, the latches make wrong decisions and the digital output code of the flash ADC will have errors. Multi-bit flash ADCs are especially prone to metastability since the input signal for each comparator decreases as the resolution of the flash ADC increases.} \]

High-speed flash ADCs usually employ pipeline stages to reduce metastability errors; however, this increases their latency. As explained in Sect. 2.2.3, the additional delay of the quantizer causes instability. Therefore, the output of a flash ADC in a ΔΣM is directly connected to the following stages such as the feedback DAC, which requires a co-design of the quantizer and the DAC. Furthermore, the performance of the ΔΣM must be simulated in the presence of metastability errors.

Metastable states of a comparator are usually very difficult to observe. Instead, the bit-error-ratio (BER), which is defined as the number of meta-stable states of a comparator per second, gives more insight at the system level. Assuming that a comparator has a pre-amplifier and a latch as shown in Fig. 2.25, the comparator’s BER can be shown to be given by [30]:

\[ \text{BER} = \frac{0.5 V_{\text{logic}}}{V_{FS} A_{pre}} \cdot e^{-\frac{A_0}{\tau} t_d}, \]

where \( V_{\text{logic}} \) is the output voltage level, \( V_{FS} \) is the full-scale input range of the comparator, \( A_{pre} \) is the gain of the pre-amplifier of the comparator, \( A_0 \) is the gain of the regenerative latch, \( \tau \) is the time constant of the latch, and \( t_d \) is the operation time of the comparator. In most cases, the comparator is only used during half of a clock period, so \( t_d \) is set to \( T_s/2 \). The metastability errors of the quantizer are shaped by the gain of the loop filter. However, the feedback DAC connected to the input of the modulator often uses a D-FF to re-time the data signal of the quantizer and enable distribution of a low-jitter clock signal. The metastability errors introduced by this D-FF at the output of the DAC, which are present at the input of the modulator, degrade the performance dramatically. In this book, the bit errors introduced by the D-FF of the feedback DAC are considered as the bit errors of the modulator. In other words, bit-errors of the modulator occur when the output of the DAC which drives the DAC current sources differs from the digital output of the modulator.

Figure 2.26a and b model the BER of the quantizer and the modulator, respectively. For each case, bit errors are introduced during the simulation with an amplitude of 1 \( LSB \) and distributed randomly through out the simulation time. The
Fig. 2.26 A basic single-loop continuous-time $\Delta \Sigma$ modulator with BER. Bit errors are introduced at the output of the quantizer (a) and the output of the DAC (b).

Simulation models the practical operation of the modulator, since only one slice of the comparator has a critical input voltage ($V_{in} < V_{tap}$) and the input voltage of the other comparators are larger than ($V_{in} > V_{tap}$), which forces them to give a correct decision. The DAC unit connected to the critical comparator has the highest chance of introducing the bit errors.

Figure 2.27 shows the SNR of a 4-bit 3rd order $\Delta \Sigma M$ in the presence of bit errors. The input signal is set to full scale and the SNR stays fairly constant for BER $< OSR^{-1}$ because the bit errors act as a white noise source at the output of the quantizer and are shaped by the NTF. However, we should note that as the BER increases, the output voltage of the integrators increases. In a practical implementation, the SNR can degrade further if the integrators of the modulator saturate. On the other hand, as shown in Fig. 2.27, the BER of the modulator degrades the SNR dramatically, because the meta-stability errors are not shaped by the modulator’s NTF. Therefore, the feedback path of the modulator must have enough gain to adequately suppress the BER below the aimed noise level.

Furthermore, a $\Delta \Sigma M$ is often followed by digital blocks such as a thermometer-to-binary decoder or a decimation filter, which use latches, and are also subject to meta-stability. Therefore, any error introduced in the digital back-end will also degrade the modulator’s SQNR.
2.3 Summary

This chapter has presented the operation of an ideal single-loop CTΔΣ modulator and described its main building blocks. The quantizer, which converts the signals into digital, is the only non-linear block of the modulator and has a phase uncertainty which is quite significant in the case of a single-bit quantizer. The non-linear behavior of the quantizer has significant effect on the modulator. Furthermore, the single-bit quantizer creates harmonic distortion and intermodulation tones. It has been shown that for a sine-wave input, the harmonic distortion and intermodulation product of a quantizer can be modeled accurately, and the presence of white noise at the input of the quantizer improves the harmonic distortion and intermodulation product at the cost of a reduced SNR.

Many types of DAC output waveforms can be implemented in a ΔΣM, but due to the focus on GHz sampling frequencies in this book, only NRZ and RZ DAC types have been analyzed. The DAC introduces a ZOH function in the feedback and its amplitude and phase response is defined by the shape of the DAC output waveform.

A ΔΣM with a 1st order loop filter is inherently stable because the loop filter has a 90° phase shift. To design a stable modulator with a higher order loop filter, the phase shift of the loop filter must be close to 90° at $f_s/2$. A complete analysis of its stability is complicated by the fact that the quantizer is a non-linear element. In most practical cases, the stability of a ΔΣM is verified by computer simulations.
System level non-idealities such as noise, linearity, metastability and excess loop delay (ELD) limit the performance of the modulator. The DAC and the first stage of the loop filter are the most dominant sources of noise because they are directly connected to the input of the modulator. Furthermore, the mismatch of a multi-bit DAC also degrades linearity. The metastability of the quantizer can be modeled as white noise added to the output of the quantizer, which then degrades SNR. If the ELD of the quantizer is too much, it will result in an unstable modulator. All the non-idealities have been analyzed by system-level simulations. In the next chapter, the system-level and detailed block-level requirements of a CTΔΣ modulator which can achieve a 125 MHz signal bandwidth with a 70 dB DR will be derived.

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