still without impacting overall system performance. Often the rest of the chip is run-
ning at a much lower frequency than the CPU as well.

Thus, each major component of the system is running at the lowest voltage consistent 
with meeting system timing. This approach can provide significant savings in power.

Mixing blocks at different $V_{DD}$ supplies adds some complexity to the design – not 
only do we need to add IO pins to supply the different power rails, but we also need a 
more complex power grid and level shifters on signals running between blocks. These 
issues are described in more detail later in the book.

## 2.4 Multi-Threshold Logic

As geometries have shrunk to 130nm, 90nm, and below, using libraries with multiple 
$V_T$ has become a common way of reducing leakage current.

Figure 2-4 shows the relationship between delay and leakage for a 90nm process. 
Figure 2-5 shows some representative curves for leakage vs. delay for a multi-$V_T$ 
library. As explained earlier, sub-threshold leakage depends exponentially on $V_T$. 
Delay has a much weaker dependence on $V_T$.

Many libraries today offer two or three versions of their cells: Low $V_T$, Standard $V_T$, 
and High $V_T$. The implementation tools can take advantage of these libraries to opti-
imize timing and power simultaneously.
Low Power Methodology Manual
For System-on-Chip Design
Flynn, D.; Aitken, R.; Gibbons, A.; Shi, K.
2007, XVI, 300 p., Hardcover